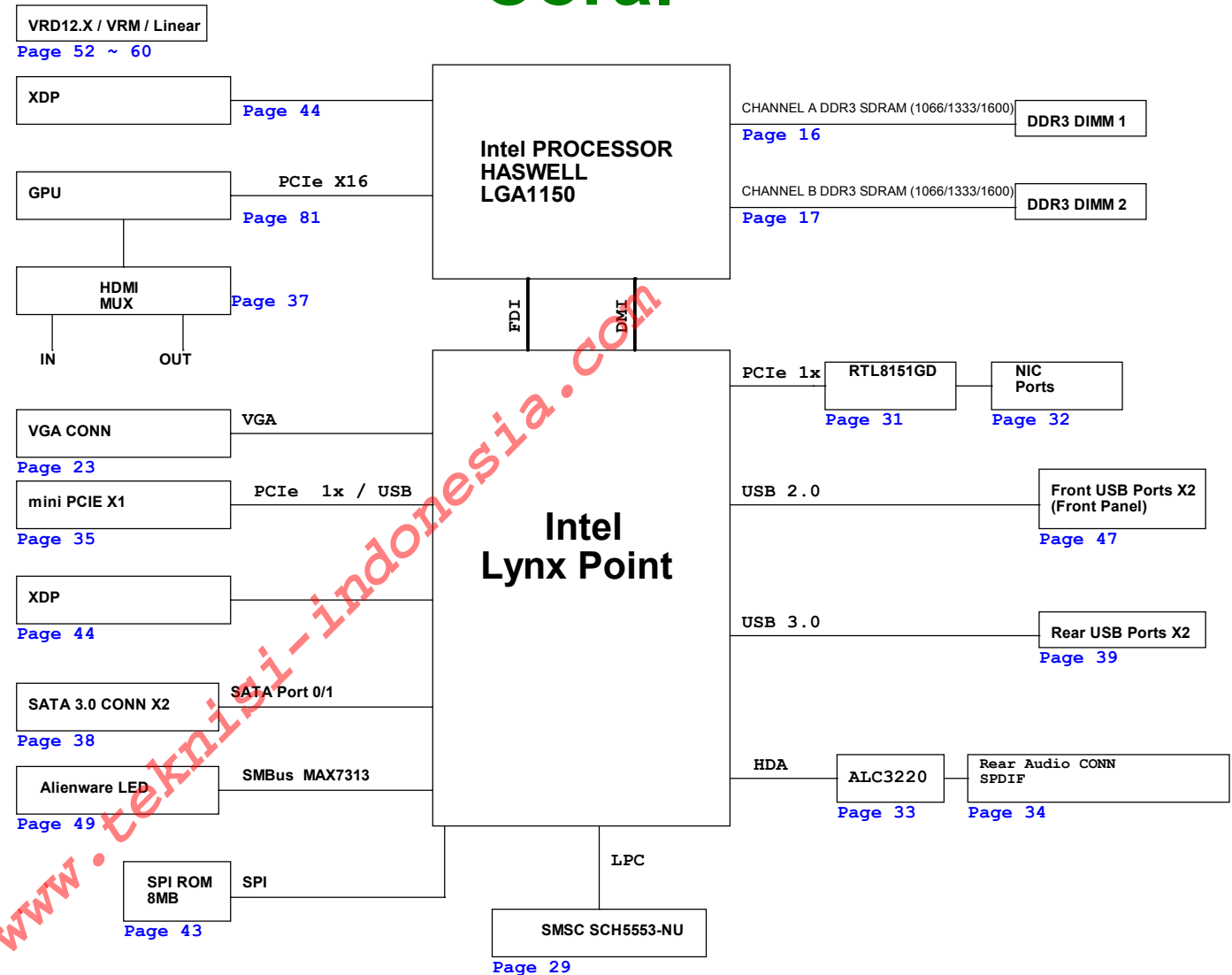


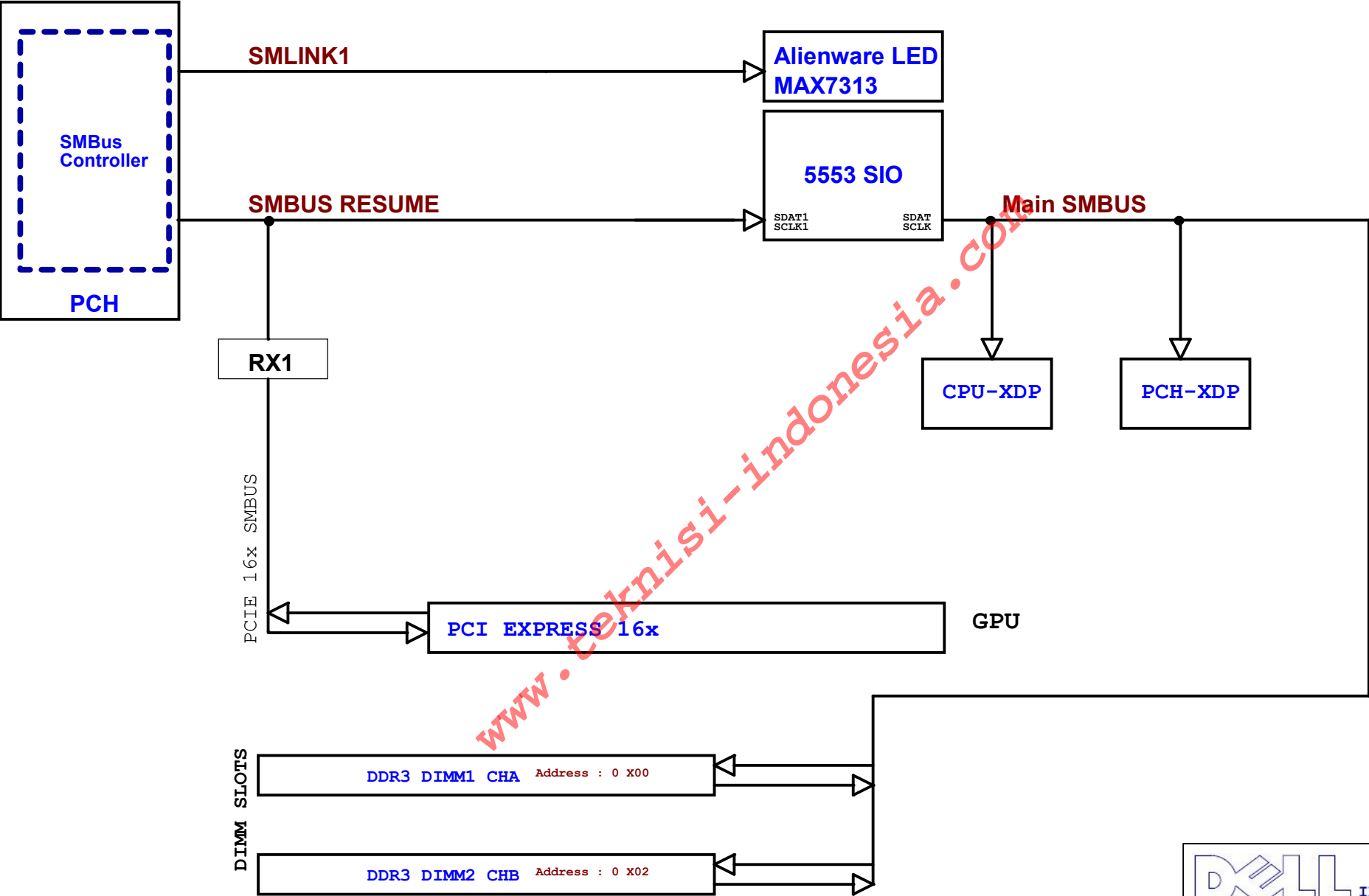
1. Index / Block diagram
2. SMBus MAP
3. Clock Distribution
4. Power Delivery Map
5. Power On Sequence
6. Reset / Power Good Map
7. Strap/IRQ/IDSel Table
8. GPIO Table
- 10-15. CPU
16. DDR3 Conn: CHA
17. DDR3 Conn: CHB
19. LABEL
- 20-27. PCH
- 29-30. SIO SCH5555-NS
- 31-32. LAN
- 33-34. AUDIO ALC3220
35. Mini PCIe /mSATA*
- 36-37. HDMI
38. SATA Conn
39. Rear USB
40. FAN
41. Thermal Sensor Conn
42. Bluetooth
43. SPI
44. XDP
45. Pilot Run Conn
46. EMI
47. Front Panel
48. Front USB3.0
49. Alienware LED
50. Alienware Light Control
52. Power Sequence
53. Adapter IN
54. 3V3 DUAL&+5VSB
55. VR MEM/VT
56. 5V S5/3V S5/3V PCIAUX
57. 1.05V PCH/1.5V PCH
58. 5V/3V/5V USB/B ATX_PG
59. Power--> Vcore PWM
60. Power--> Vcore Driver
62. Change list
63. Table of Contents
64. Block Diagram
65. PCI-Express Gen3 x16 Inter
- 66-71. Frame Buffer
72. FBVDDQ Decoupling Caps
73. NVVDD Decoupling Caps
- 74-78. IFPA_B/IFPC/IFPD/IFPDEF/IFPDG
79. DACA
80. VBIOS ROM,XTAL, External S
81. GPIOs, Thermal Sensor, I2C
83. Straps
- 84-85. NVVDD
86. FBVDDQ
87. PEX_VDD1.05V
88. Miscellaneous Voltage Rail
89. PEX_VDD Switcher
90. Power Enables-1
91. Power Enables and FBVDDQ




DESIGN	CHECK	APPROVE
Steven	Sam	Sdiu

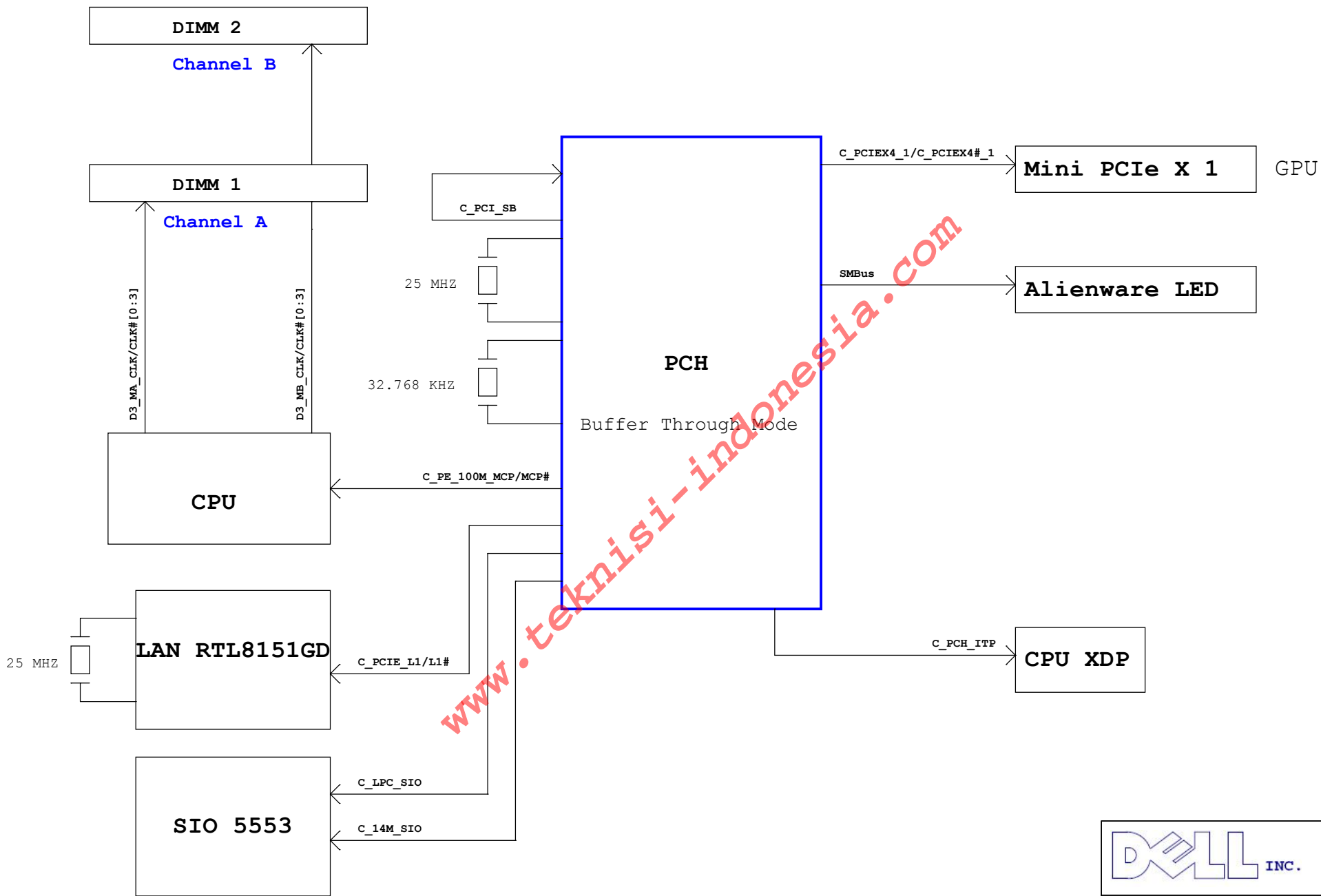
DELL INC.	
Title Index / Block diagram	
DWG NO Coral	Rev X01
Date: Tuesday, August 12, 2014 Sheet 1 of 91	

SMBUS DIAGRAM

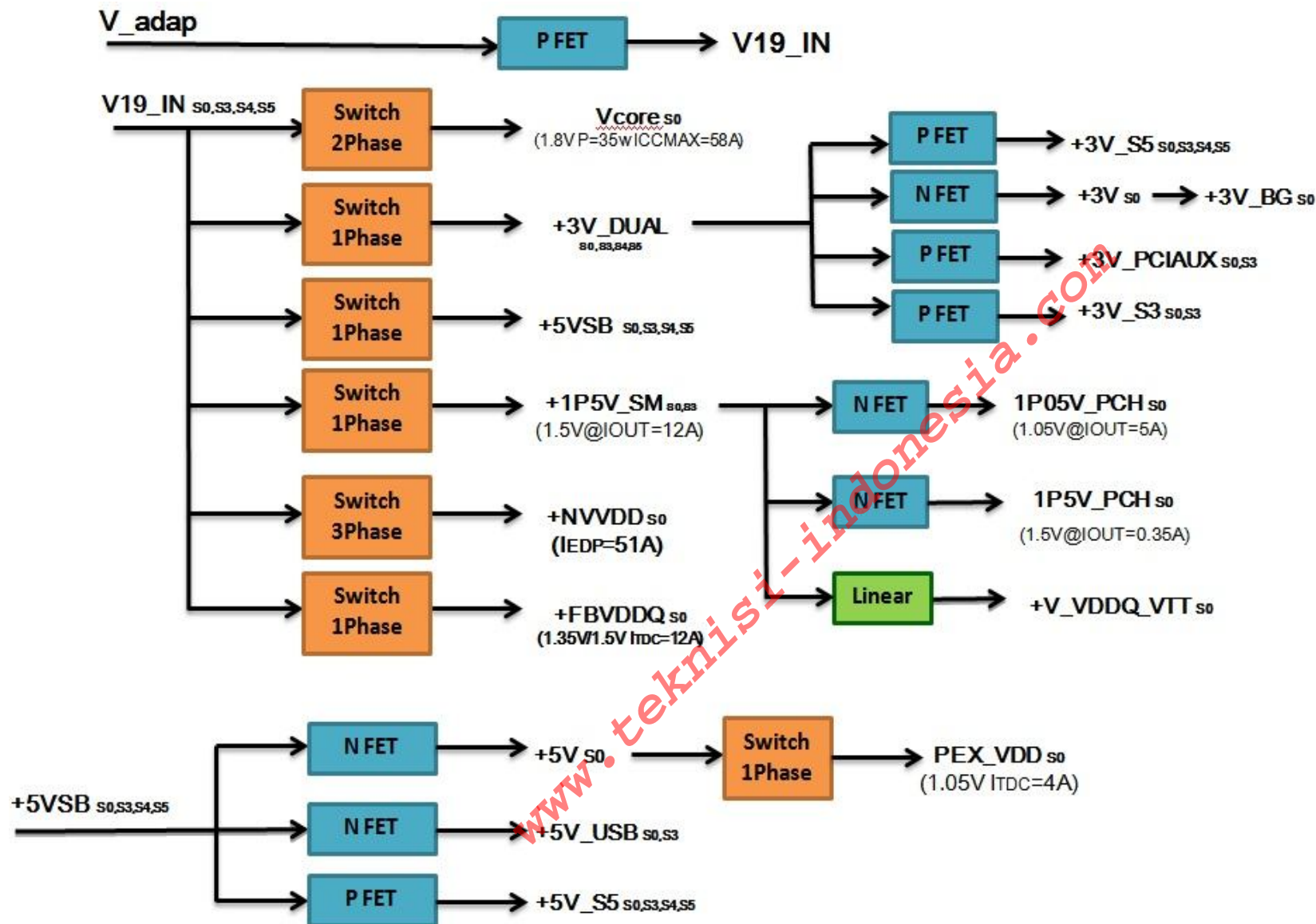


**INC.**

Title		BLOCK DIAGRAM	
DWG NO	Coral		Rev
		X01	
Date:	Tuesday, August 12, 2014	Sheet	2 of 91

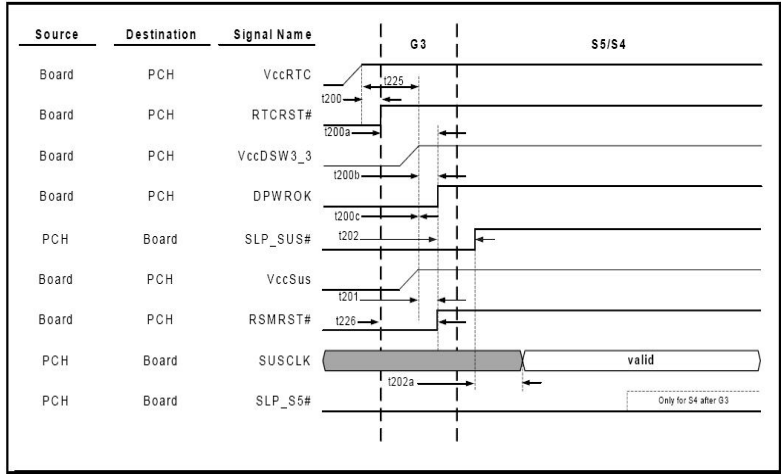


POWER DELIVERY MAP

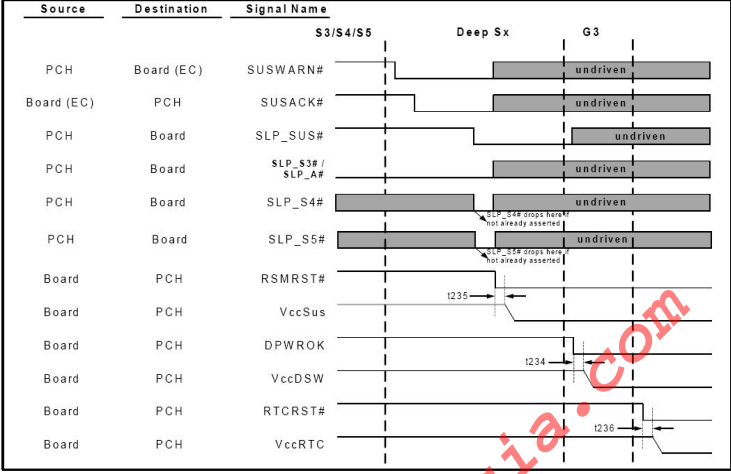


POWER ON Timing Diagram

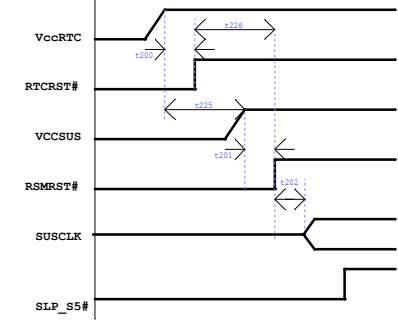
G3 --> S4/S5 (with Deep Sleep support)



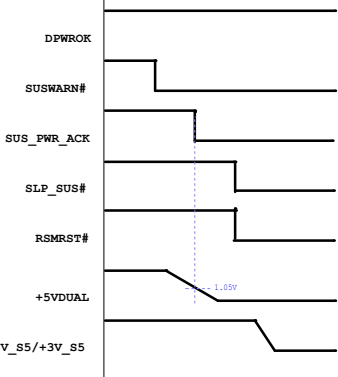
Sx --> Deep S4/S5 -->G3



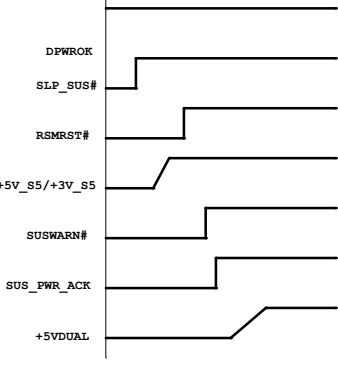
G3 to S4/S5 Timing Diagram



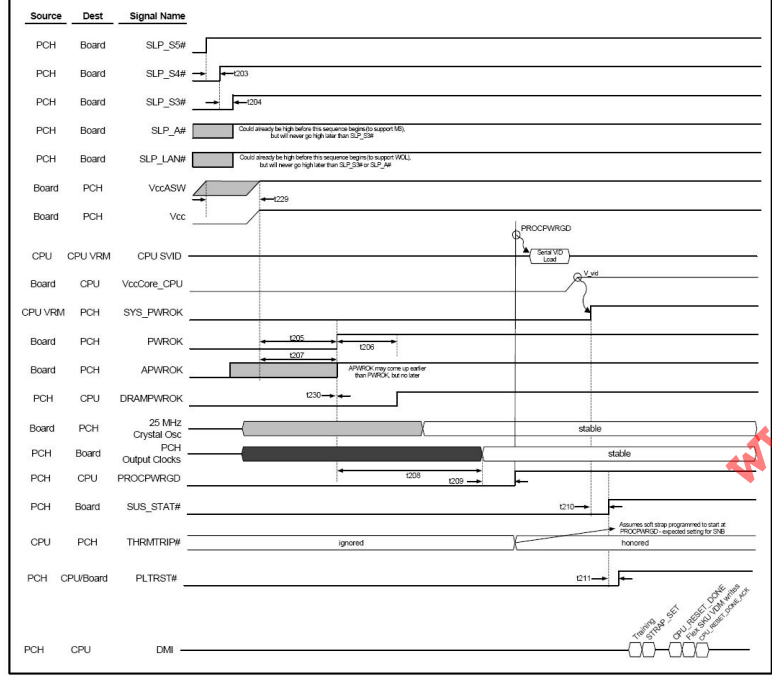
Deep Sleep Entry



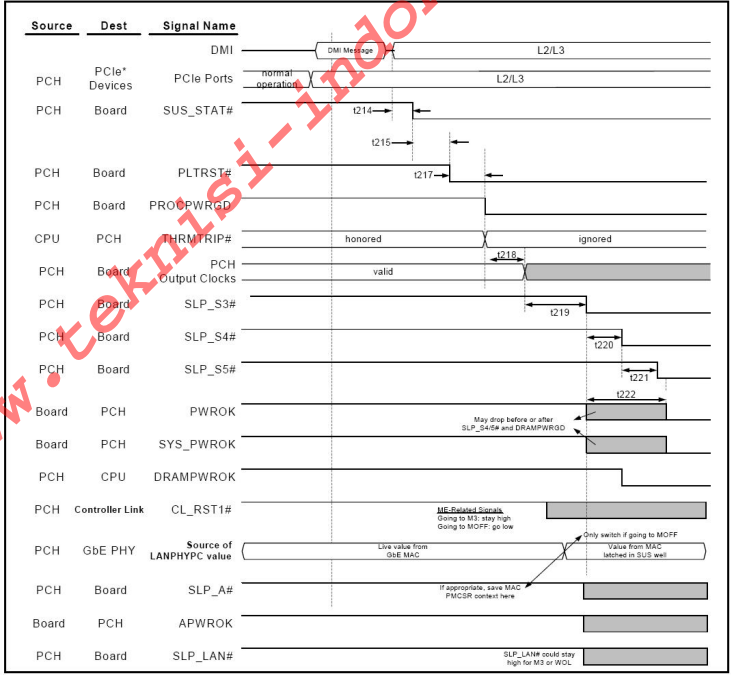
Deep Sleep Exit



S5 --> S0



S0 --> S5



STRAPPING Table

PCH side

Table 36-18. Strapping Signals (Sheet 1 of 2)

Name	Type	Recommendations	Reason/Impact
SPKR	I	Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2k-10k Ohm weak pull-up resistor.	
INIT3_3V#	I	Do not pull low.	
GPI055	I/O	Default Mode: Internal pull-up. Top Block Swap Mode: Connect to ground with 4.7k Ohm weak pull-down resistor.	
SATA1GP/ GPI019, GPI051	I/O	Default (SPI) Left both SATA1GP/GPI019 and GPI051 floating. No pull up required. Boot from PCI Connect SATA1GP/GPI019 to ground with 1k Ohm pull-down resistor. Leave GPI051 Floating. Boot from LPC Connect both SATA1GP/GPI019 and GPI051 to ground with 1k Ohm pull-down resistor.	If LPC is selected BIOS may still be placed on LPC, but all platforms with PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.
GPI053	I/O	Do not pull low. Connect to ground with 1k Ohm pull-down resistor.	ES1 strap for server platform ONLY
HDA_SDO	I/O	Default Do not pull high. Disable ME in Manufacturing Mode Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.	Flash descriptor Override
SPI_MOSI	I/O	Internal weak pull down. Do not pull high.	DMI RX Termination Voltage
SAAT3GP/ GPI037	I/O	Enable TLS: Pull up with 1k Ohm to VccSus3.3. Default (Disable TLS): Leave NC. Internal pull down.	TLS confidentiality
GPI08	I/O	Internal weak pull up. Do not pull low.	

Table 36-18. Strapping Signals (Sheet 2 of 2)

Name	Type	Recommendations	Reason/Impact
GPI062/ SUSCLK	I/O	Internal weak pull up. Do not pull low.	On die PLL voltage regulator
GPI036	I/O	Internal weak pull down. Do not pull high.	
DDPB_CTRL_DATA DDPC_CTRL_DATA DDPD_CTRL_DATA		Straps for digital ports B, C and D. For DisplayPort* - Should be pulled to 3.3V through a 2.2k ohms resistor to configure digital port. For DVI/HDMI configuration, the signal should be routed through the level shifter to the display connector. The signal is pulled to 3V before the level shifter and 5V before the display connector through a 2.2k ohms resistor. This signal should always be routed longer than SDVO/DDPC_CTRLCLK by an inch. For DVI/HDMI configuration with the Cost Reduced level shifter, the signal should be routed through the pass gate sourced from 3.3V voltage to the display connector. The signal is pulled to 3V before the pass gate and 5V before the display connector through a 2.2k ohms resistor. This signal should always be routed longer than SDVO/DDPC_CTRLCLK by an inch.	

CPU side

Signal Name	Description	Direction/ Buffer Type
CFG[19:0]	Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. <ul style="list-style-type: none"> CFG[1:0]: Reserved configuration lane. A test point may be placed on the board for this lane. CFG[2]: PCI Express* Static x16 Lane Numbering Reversal. <ul style="list-style-type: none"> x1 = Normal operation x0 = Lane numbers reversed. CFG[3]: PCI Express* Static x4 Lane Numbering Reversal. <ul style="list-style-type: none"> x1 = Normal operation x0 = Lane numbers reversed. CFG[4]: Reserved configuration lane. A test point may be placed on the board for this lane. CFG[6:5]: PCI Express* Bifurcation:¹ <ul style="list-style-type: none"> x00 = 1 x8, 2 x4 PCI Express* x01 = reserved x10 = 2 x8 PCI Express* x11 = 1 x16 PCI Express* CFG[19:7]: Reserved configuration lanes. A test point may be placed on the board for these lanes. 	I CMOS

Strapping Options Flash

GNT1#	SATA1GP/GPI019	Routing
0	0	Flash Cycles Routed to LPC
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to SPI

Table 34-6. PCH Digital Display Strapping Signals

Checklist Item	Recommendations	Direction	Comments
DDPX_CTRLDATA	Straps for digital port B, C and D. For DisplayPort* - Should be pulled to 3.3V through a 2.2K W resistor to configure digital port. For DVI/HDMI configuration, the signal should be routed through the level shifter to the display connector. The signal is pulled to 3V before the level shifter and 5V before the display connector through a 2.2KW resistor. This signal should always be routed longer than DDPC_CTRLCLK by an inch. For DVI/HDMI configuration with the Cost Reduced level shifter, the signal should be routed through the pass gate sourced from 3.3V voltage. The signal is pulled to 3V before the pass gate and 5V before the display connector through a 2.2KW resistor and a Schottky diode. This signal should always be routed longer than DDPC_CTRLCLK by an inch. Also ensure schottky diode is not shared with DDPC_CTRLCLK.	BI	

SIO SMSC5555

PIN NAME	NET		Strapping description
GP070 / PWM4 (PIN127)	O_SPEAKER	1	Diag_En Disable
		0	Diag_En Enable DEFAULT



Title GPIO/IRQ/IDSEL Table		
DWG NO Coral	Rev B00	
Date: Tuesday, August 12, 2014	Sheet 7 of 91	

PIN OUT		Signal Name		EX-PU/PD	'Current Usage	Programming Function	PCH GPIO Summary																														
PIN OUT		Power well	Buffer Type	Signal Name			I/O/NU/Native/Strapping																														
4	V3_55	I04		NC	NA		Native	NA																													
5	V3_55	I04		NC	NA		Native	NA																													
7	V3_55	I04		NC	NA		Native	NA																													
8	V3_55	I04		NC	NA		Native	NA																													
70	V3_55	I04		S_SUSWARN#	NA		Native	NA																													
22	V3_55	I04		O_PECU_REQ#	10k pull-up to +3V		Native	NA																													
25	V3_55	I08		O_YELLOW#	499 pull-up to +5V_55		Native	NA																													
26	V3_55	I08		O_GREEN#	499 pull-up to +5V_55		Native	NA																													
27	V3_55	I08		S_SML1DATA	2.2k pull-up to +3V_55		Native	NA																													
28	V3_55	I08		S_SML1CLK	2.2k pull-up to +3V_55		Native	NA																													
30	V3_55	I04		O_DPWR0K	10k pull-down to GND		Native	NA																													
35	V3_55	I04		TM1L_SHIFT	9.2k pull-up to +3V_55 330k pull-down to GND (dummy)		I	1: default 0: Tmen down adjustment																													
36	V3_55	I04		O_PWRBTN#N	1k pull-up to +3V_DUAL (dummy)		Native	NA																													
38	V3_55	LW0D24		H_PROCHOT#	510hm pull-up to H_CPU_VCCIO_RIGHT		Native	NA																													
39	V3_55	I04		O_SEM_CPUFAN	1k pull-up to +3V		Native	NA																													
40	V3_55	I04		O_SEM_CHAFAN	1k pull-up to +3V		Native	NA																													
41	V3_55	I04		NC	NA		NU	NA																													
49	V3_55	I04		O_CPUFAN_PWM	4.7k pull-up to +3V		Native	NA																													
50	V3_55	I04		O_CHAFAN_PWM	4.7k pull-up to +3V		Native	NA																													
51	V3_55	I04		NC	NA		NU	NA																													
52	V3_55	I04		O_FP_CBL_DET#	9.2k pull-up to +3V_55		I	1: default 0: power switch cable plugged																													
53	V3_55	I04		X_PLTRST_PCIE_SLOT#	NC		Native	NA																													
54	V3_55	I04		NC	NA		NU	NA																													
55	V3_55	OD4		O_PSD0#	4.7k pull-up to +5VSB		Native	NA																													
56	V3_55	I04		O_AUD_PCSPKR_DET#	8.2k pull-up to +3V_55		I	1: default 0: PC speaker cable plugged																													
58	V3_55	I04		O_SUS_3V_F_ON	NA		Native	NA																													
59	V3_55	I04		PWR0D_3V	NA		Native	NA																													
60	V3_55	O4		O_RSMRST#	NA		NU	NA																													
69	V3_55	I04		NC	NA		NU	NA																													
72	V3_55	I08		NC	NA		NU	NA																													
74	V3_55	I08		NC	NA		NU	NA																													
77	V3_55	I04		O_PME#	10k pull-up to +3V_55		Native	NA																													
78	V3_55	I04		NC	NA		NU	NA																													
98	V3_55	I04		O_DCD1#_R	NA		Native	NA																													
99	V3_55	I04		O_DCD1#_R	NA		Native	NA																													
100	V3_55	I04		O_RXD1#_R	NA		Native	NA																													
101	V3_55	I04		O_RTS1#_R	10k pull-up to +3V		Native	NA																													
102	V3_55	I08		O_TXD1#_R	10k pull-up to +3V		Native	NA																													
103	V3_55	I04		O_CTS1#_R	NA		Native	NA																													
104	V3_55	I04		O_DTR1#_R	NA		Native	NA																													
105	V3_55	I04		O_R1#_R	NA		Native	NA																													
107	V3_55	I04		NC	NA		Native	NA																													
108	V3_55	I04		NC	NA		Native	NA																													
109	V3_55	I04		NC	NA		Native	NA																													
110	V3_55	I04		O_PWR2_PBSHT	10k pull-up to +3V		Native	NA																													
111	V3_55	I08		O_ML1_REG_PG	10k pull-up to +3V		Native	NA																													
112	V3_55	I04		NC	NA		Native	NA																													
113	V3_55	I04		O_MEM1_REG_PG	10k pull-up to +3V		Native	NA																													
114	V3_55	I04		NC	NA		Native	NA																													
120	V3_55	I04		O_JB1_RST#	10k pull-up to +3V		Native	NA																													
121	V3_55	I04		O_A20GATE	10k pull-up to +3V		Native	NA																													
124	V3_55	I04		S_SLP_55#	NA		Native	NA																													
127	V3_55	I04		O_SPEAKER	8.2k pull-up to +3V_55(dummy) 8.2k pull-down to GND		Native	NA																													
128	V3_55	I04		S_SLP_55#	NA		Native	NA																													
75	V3_55	I04		O_SUS_5VON	22k pull-up to +5VSB		Native	NA																													
76	V3_55	I04		O_SUS_3V_ON	NA		Native	NA																													
84	V3_55	I012		NC	NA		Native	NA																													
85	V3_55	I012		NC	NA		Native	NA																													
86	V3_55	I012		NC	NA		Native	NA																													
87	V3_55	I012		NC	NA		Native	NA																													
88	V3_55	I012		NC	NA		Native	NA																													
89	V3_55	I012		NC	NA		Native	NA																													
90	V3_55	I012		NC	NA		Native	NA																													
91	V3_55	I012		NC	NA		Native	NA																													
63	V3_55	I04		NC	NA		Native	NA																													
64	V3_55	I04		NC	NA		Native	NA																													
65	V3_55	I04		NC	NA		Native	NA																													

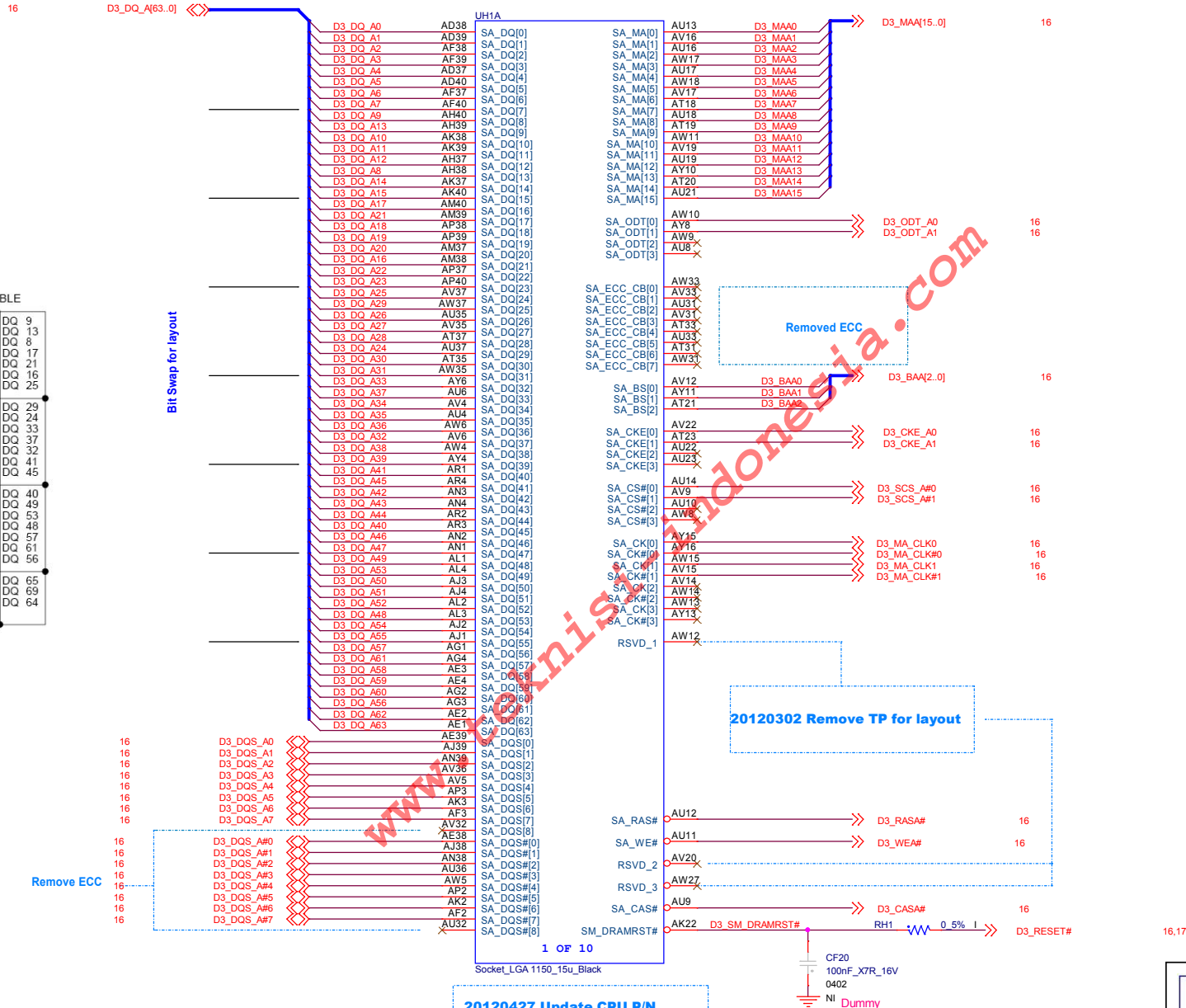
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Title
Block1

DWG NO Coral	Rev B00
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DDR3 CH-A



CPU-1: DDR3_CHA

DWG NO **Coral** Rev **B00**

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17 D3_DQ_B[63..0] 

Bit Swap for layout



DWG NO

B00

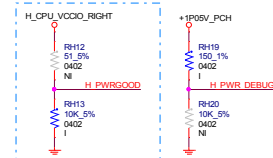
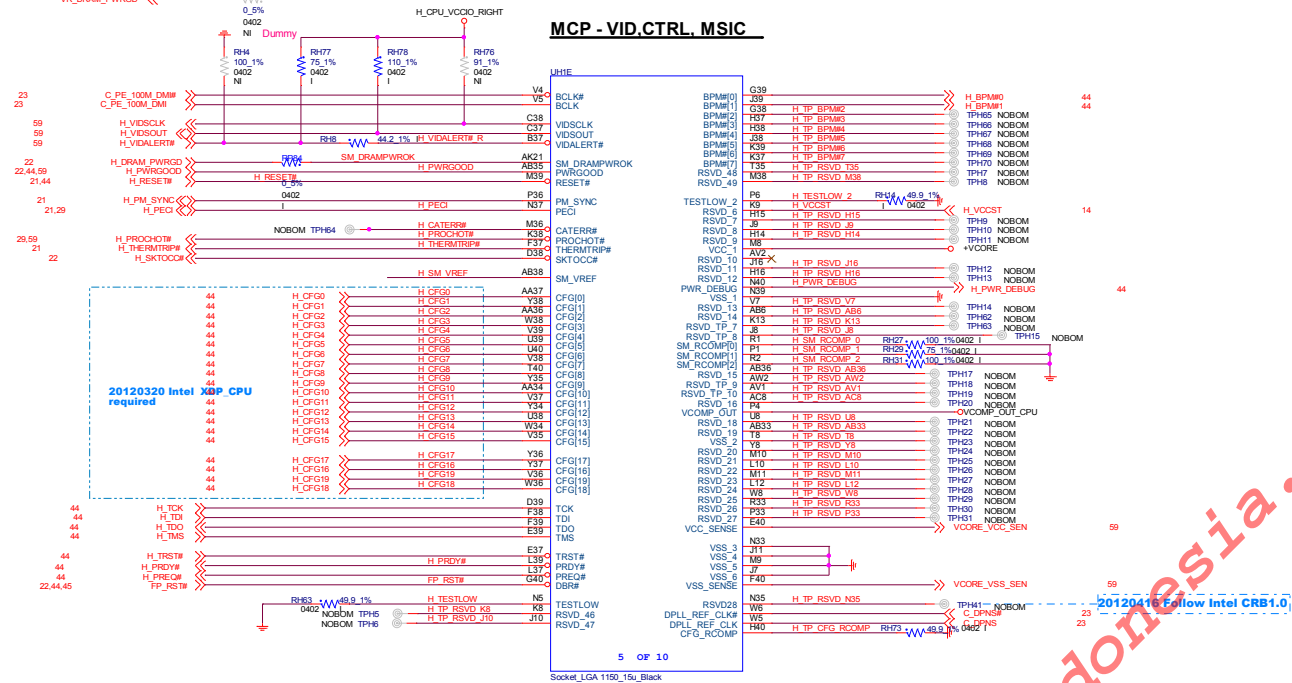
Date: Tuesday, August 12, 2014

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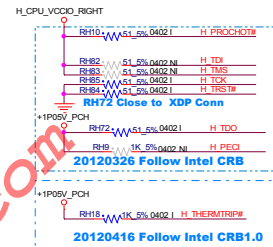
VR_DRAM_PWRGD << VR_DRAM_PWRGD_RPH1 SM_DRAMPWRCK

H_CPU_VCCIO_RIGHT

MCP - VID_CTRL, MSIC

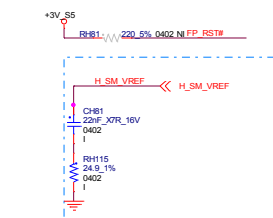


20120416 Follow Intel CRB1.0



20120326 Follow Intel CRB

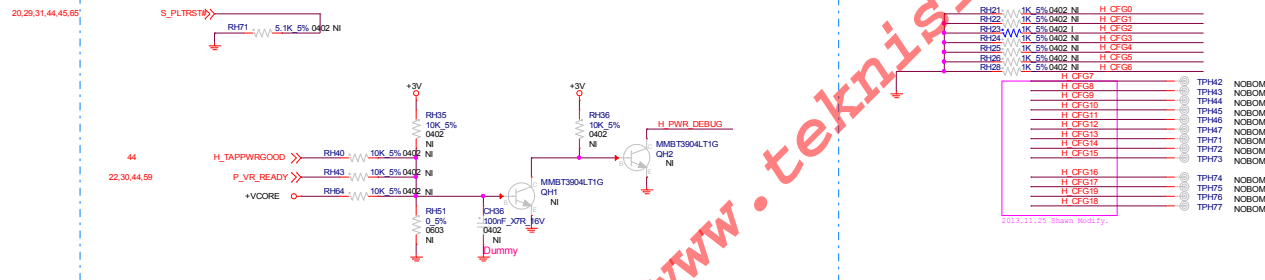
20120416 Follow Intel CRB1.0

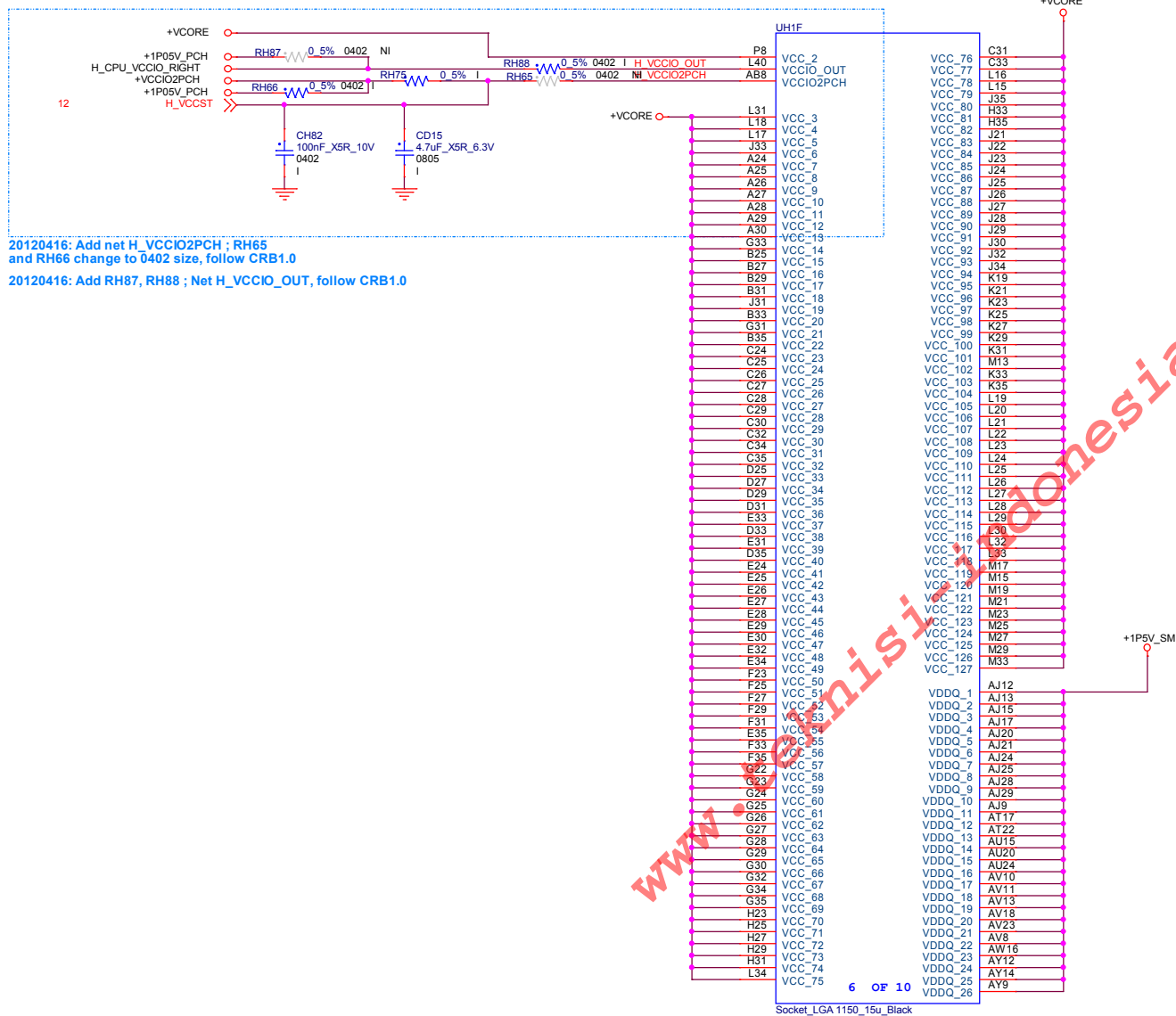


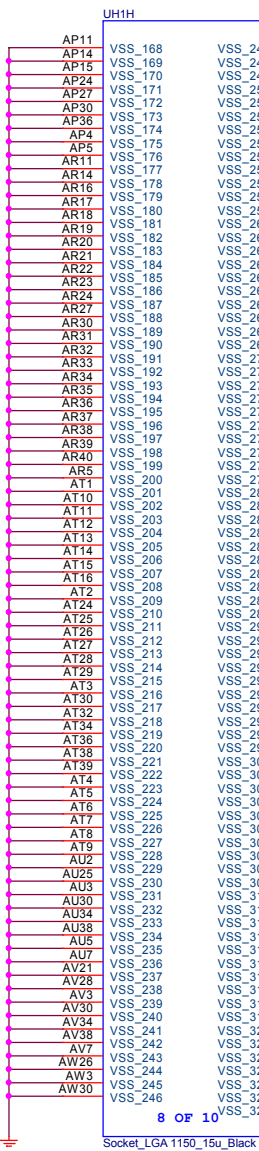
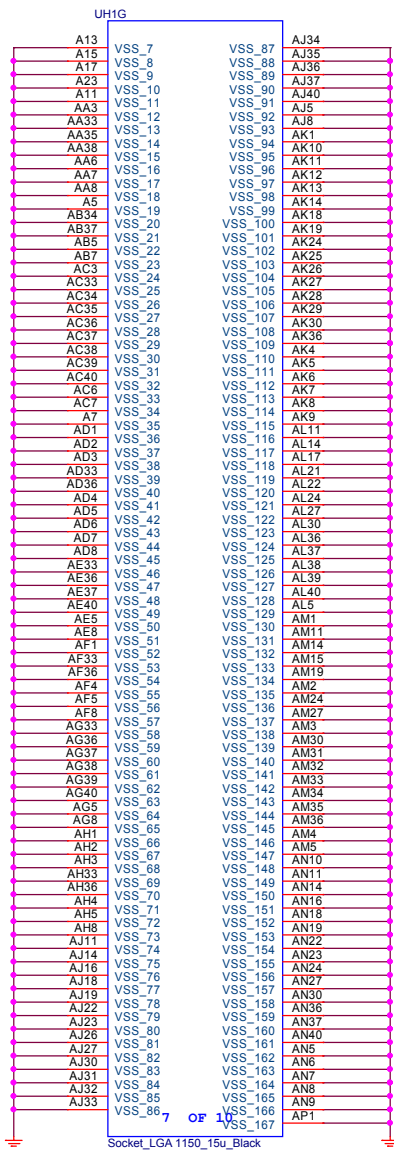
CPU REST CIRCUITRY

Ensure timings and edge rates are met on PLTRST# going to processor.

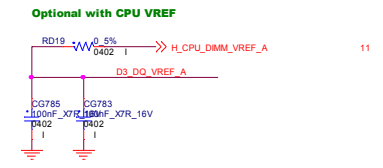
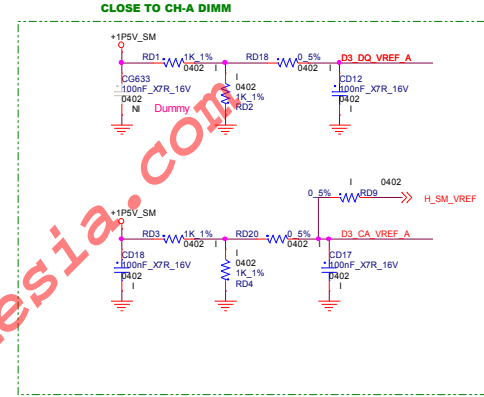
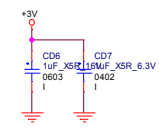
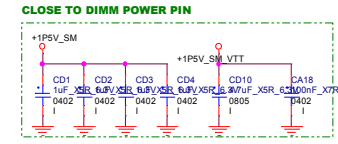
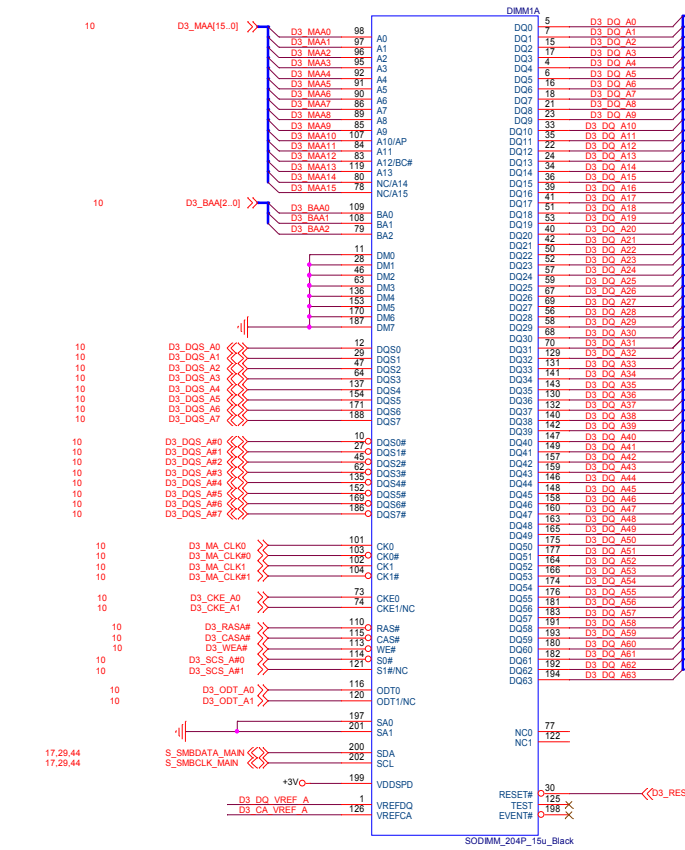
Check with Intel for this circuit necessary ??

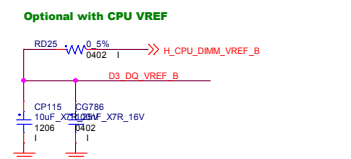
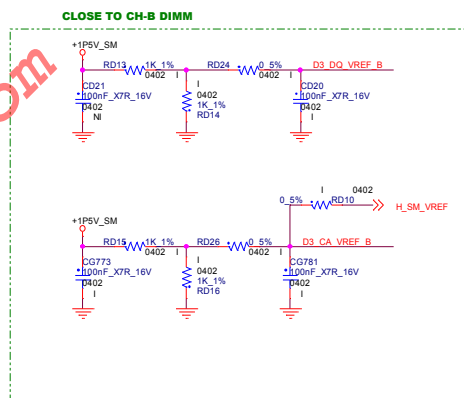
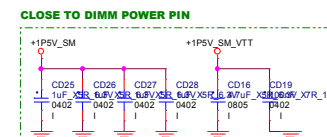
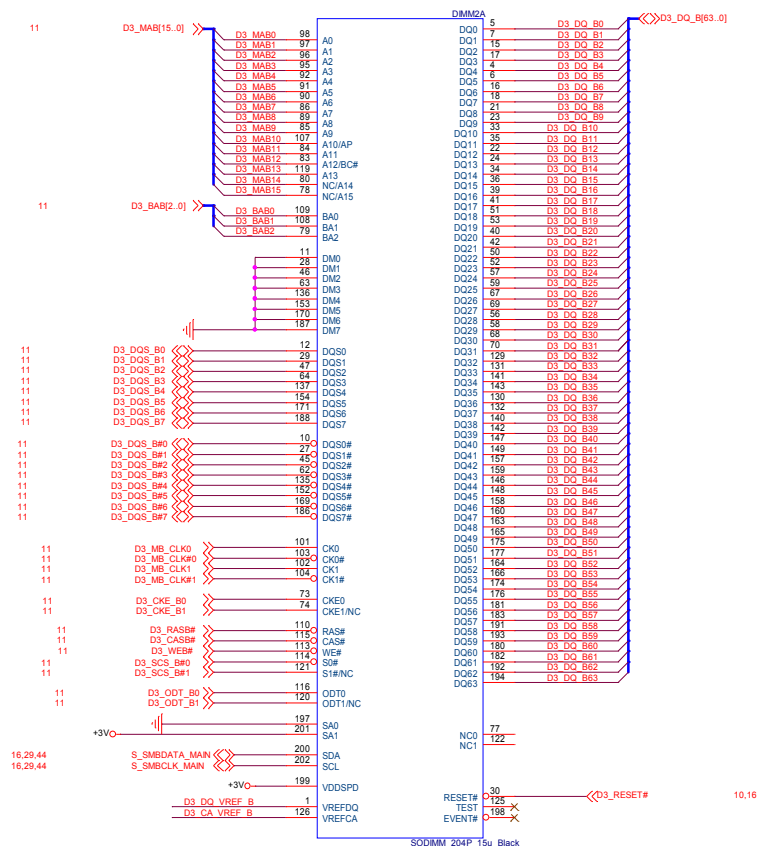






CHANNEL A BANK 1
SMB ADDRESS:000





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Title		
Block2		
DWG NO	Rev	
Coral	B00	
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Label

MTG_HDD_1 MTG_HDD_2

JP2

1	top-DIFF_5mil/7mil/5mil+
2	top-DIFF_5mil/7mil/5mil-

Header_1X2_GF 85+/-15%(Differential)-----L1

Dummy

JP3

1	top-DIFF 4mil/10mil/4mil+
2	top-DIFF 4mil/10mil/4mil-

Header_1X2_GF 100 +/-15%(Differential)-----L1

Dummy

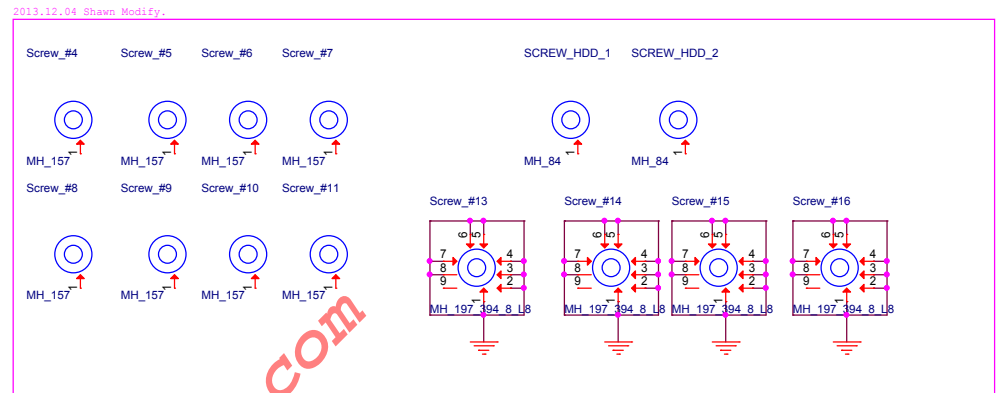
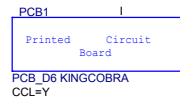


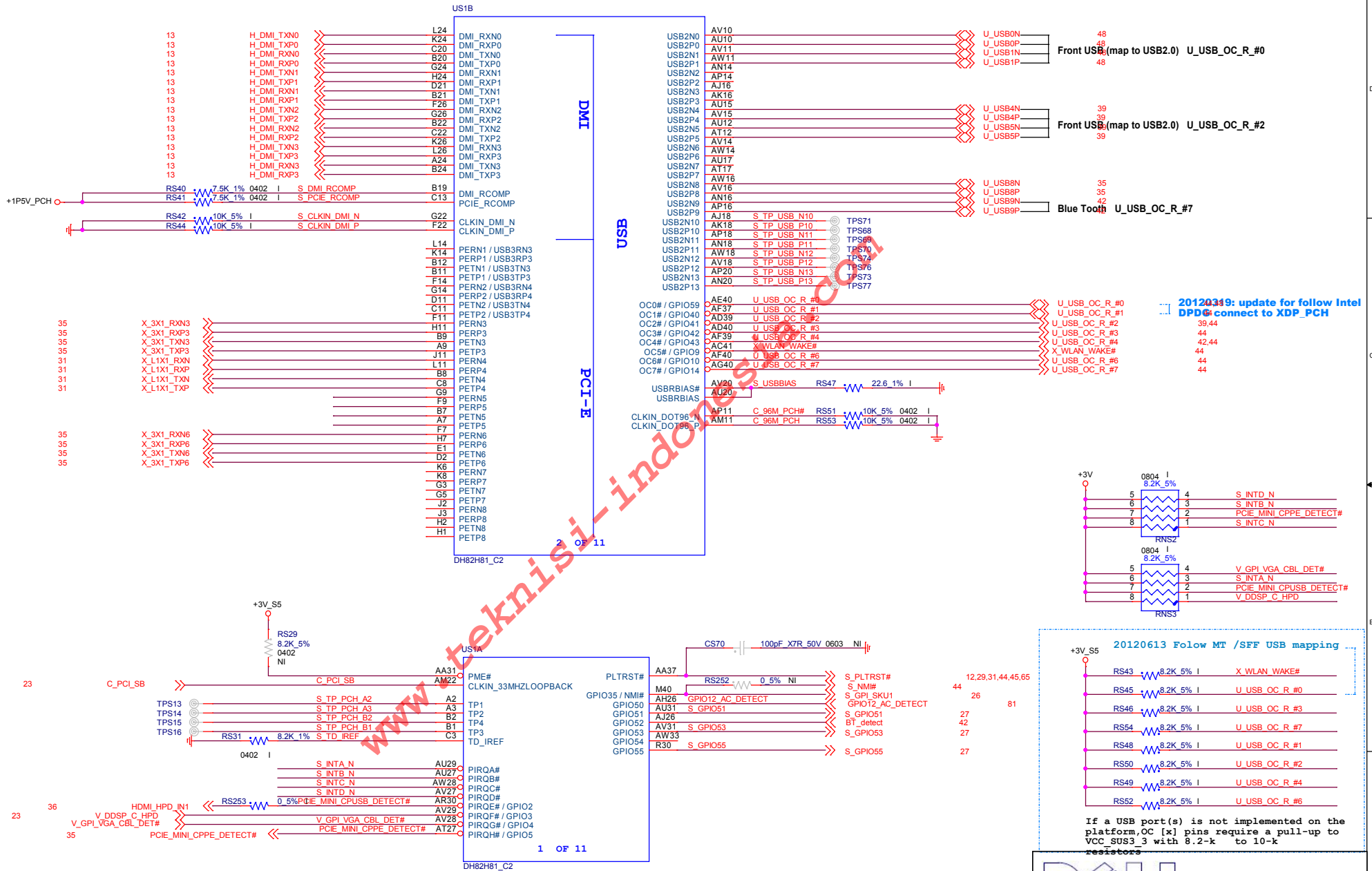
Diagram showing six identical circular components labeled FM1 through FM6, each with a blue center, a red dot, and the word "OPTICS" below it.

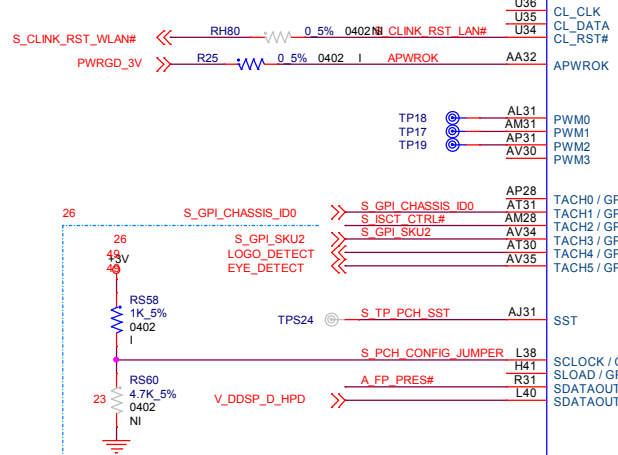
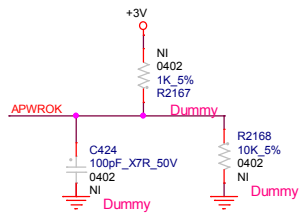


Title	LABEL
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DWG NO	<i>Coral</i>	Rev	B00
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US1C

U36
U35
U34
U33
U32
U31
U30
U29
U28
U27
U26
U25
U24
U23
U22
U21
U20
U19
U18
U17
U16
U15
U14
U13
U12
U11
U10
U9
U8
U7
U6
U5
U4
U3
U2
U1

APWROK

PWM0
PWM1
PWM2
PWM3

AP28
AT31
AM28
AV34
AT30
AV35

S_GPIO_CHASSIS_ID0
S_GPIO_SKU2
LOGO_DETECT
EYE_DETECT

S_TP_PCH_SST

S_PCH_CONFIG_JUMPER

A_FP_PRES#

V_DDSP_D_HPD

SCLOCK / GPIO22
SLOAD / GPIO38
SDATAOUT0 / GPIO39
SDATAOUT1 / GPIO48

TP18
TP17
TP19

AL31
AM31
AP31
AV30

APWROK

APWROK

APWROK

APWROK

APWROK

APWROK

APWROK

APWROK

APWROK

APWROK

GLINK
FAN
SATA

GPIO

HOST

3 OF 11

DH82H81_C2

SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
SATA_RXN1
SATA_RXP1
SATA_TXN1
SATA_TXP1

SATA_RXN2
SATA_RXP2
SATA_TXN2
SATA_TXP2
SATA_RXN3
SATA_RXP3
SATA_TXN3
SATA_TXP3

SATA_RXN4 / PERP1
SATA_RXP4 / PERP1
SATA_TXN4 / PETN1
SATA_TXP4 / PETN1
SATA_RXN5 / PERP2
SATA_RXP5 / PERP2
SATA_TXN5 / PETN2
SATA_TXP5 / PETN2

CLKIN_SATA_N
CLKIN_SATA_P
CLKIN_SATA_P

SATALED#
SATA_RCOMP

SATA0GP / GPIO21
SATA1GP / GPIO19
SATA2GP / GPIO36
SATA3GP / GPIO37
SATA4GP / GPIO16
SATA5GP / GPIO49

EDP_BKLTCTL
EDP_BKLTEN
EDP_VDDEN

TP14
RCIN#
SERIRQ
THRMTTRIP#
PECI
PMSYNCH
PLTRST_PROCH

TP14
RCIN#
SERIRQ
THRMTTRIP#
PECI
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PLTRST_PROCH

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PLTRST_PROCH

TP14
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SERIRQ
THRMTTRIP#
PECI
PMSYNCH
PLTRST_PROCH

20120305: delete TPS78, TPS79 for layout request

S CLIN SATA N
S CLIN SATA P

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S CLIN SATA P

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Update by Jose on 9/14

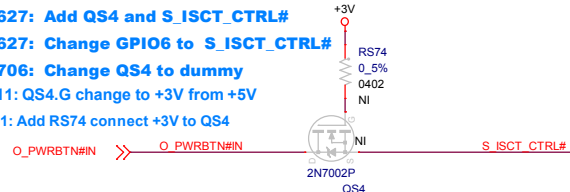
20120627: Change GPIO6 to S_ISCT_CTRL#

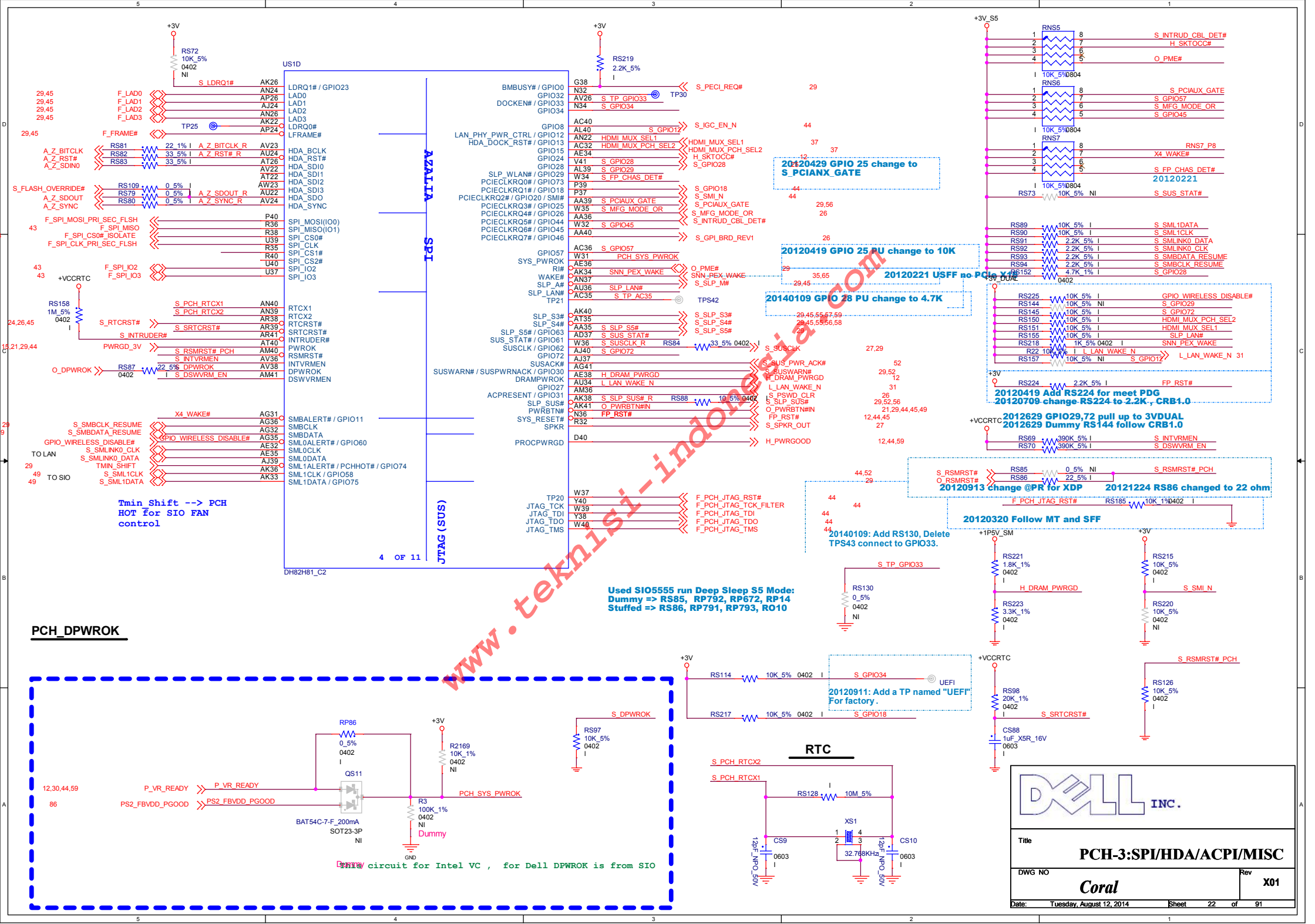
20120320: update for follow Intel DPDS connect to XDP_PCH

For Mini PCIe / mSATA Strapping

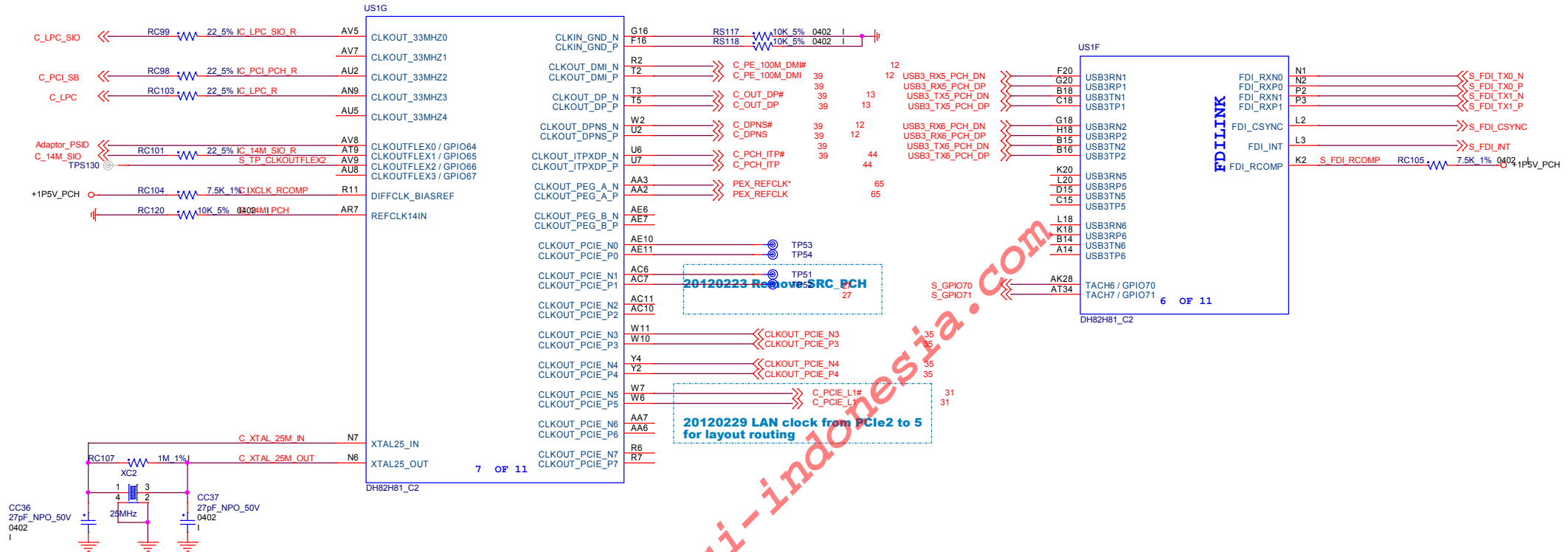
If CPU RESET CIRCUIT pop. RS71 need to Dummy

20120627: Add QS4 and S_ISCT_CTRL#
20120627: Change GPIO6 to S_ISCT_CTRL#
20120706: Change QS4 to dummy
20120911: QS4.G change to +3V from +5V
20120911: Add RS74 connect +3V to QS4

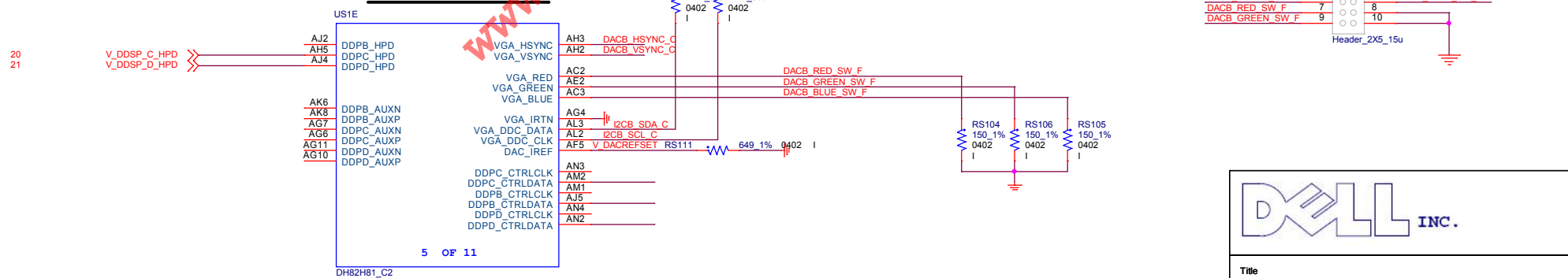


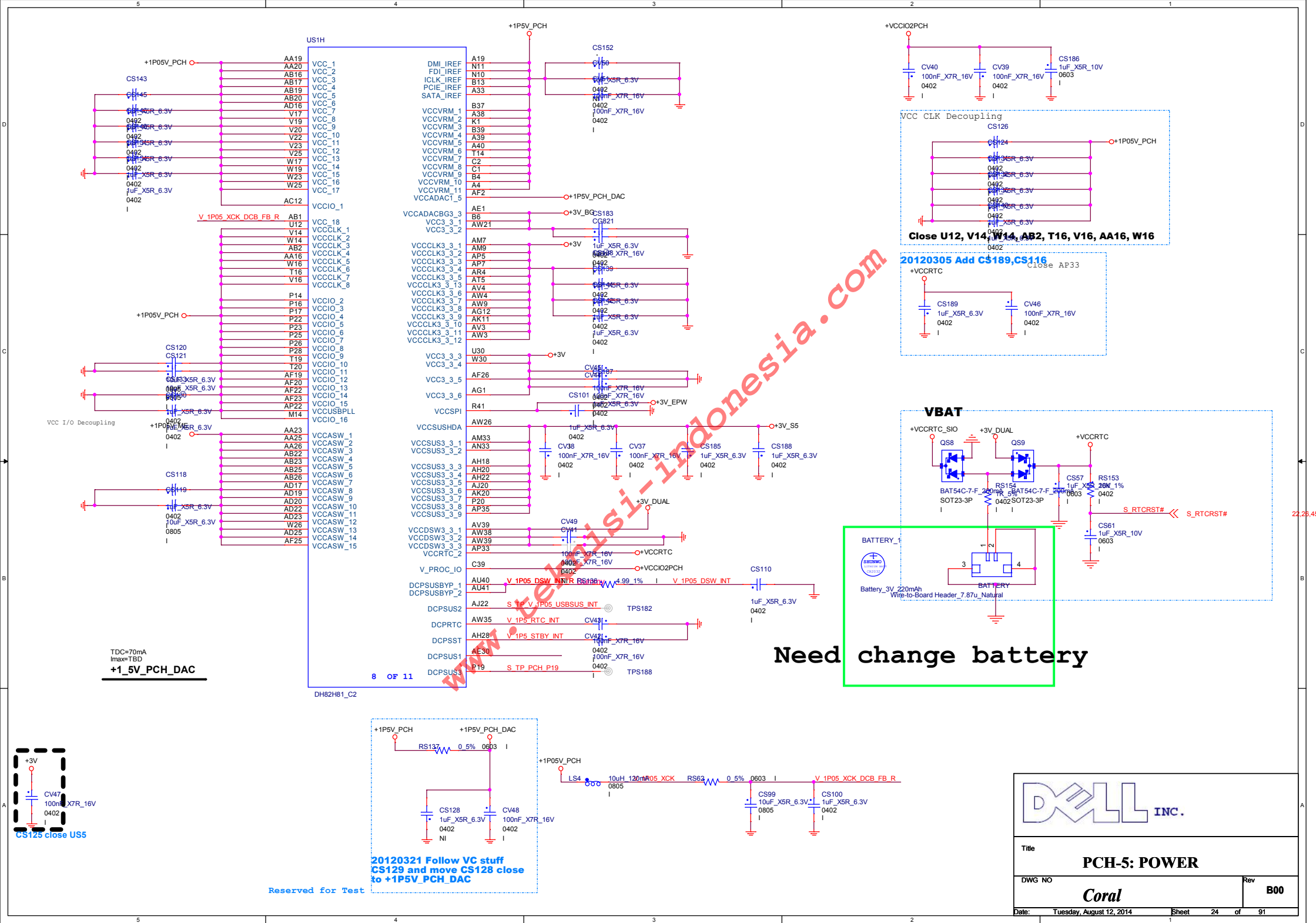


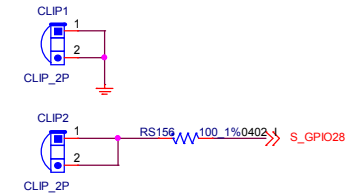
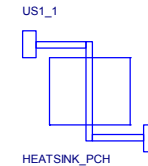
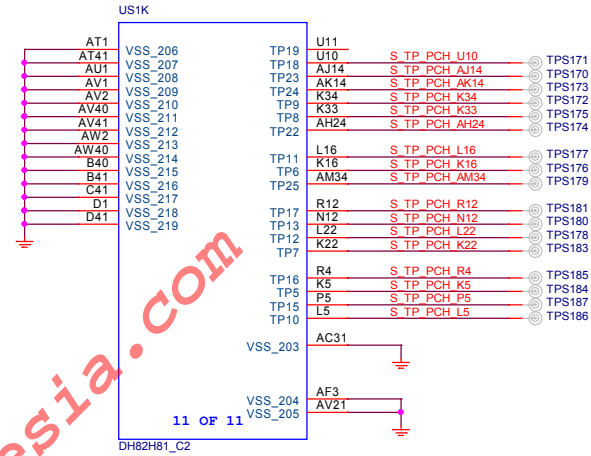
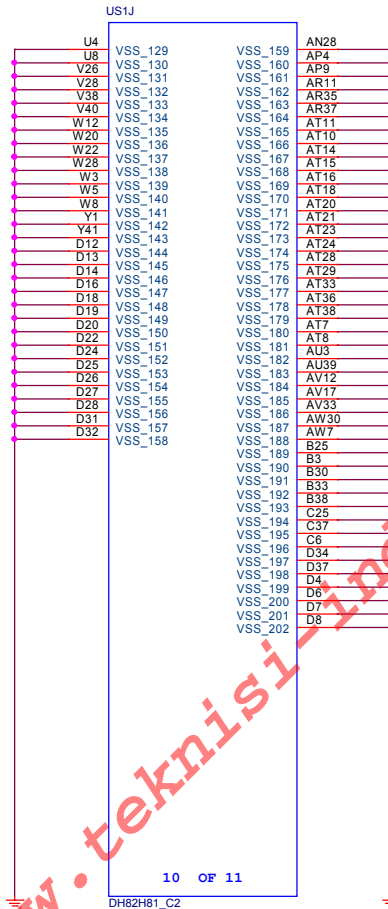
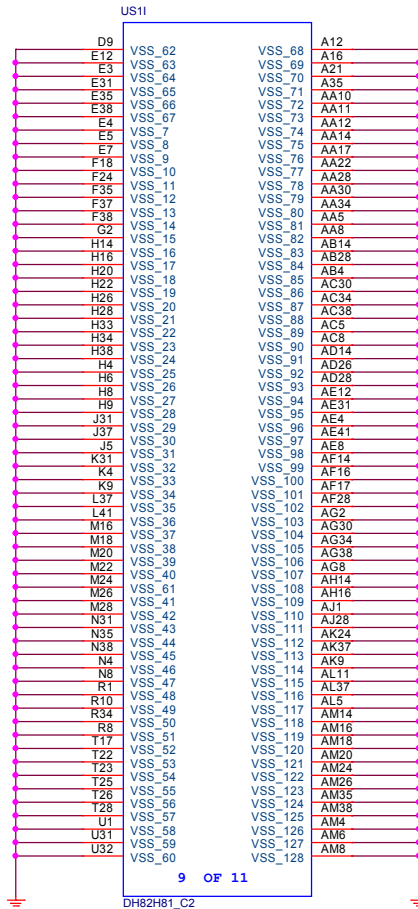
PCH - CLOCK DISTRIBUTION



PCH - DP AND RGB







Title

PCH-6: GND

DWG NO

Coral

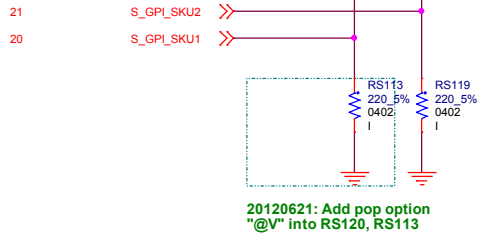
Rev

B00

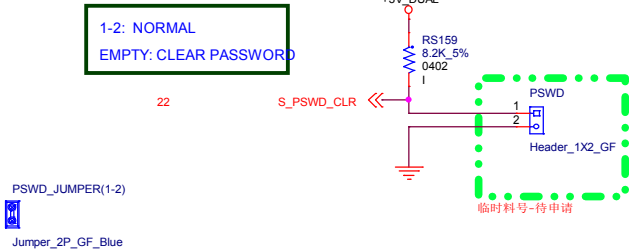
Date: Tuesday, August 12, 2014

Sheet 25 of 91

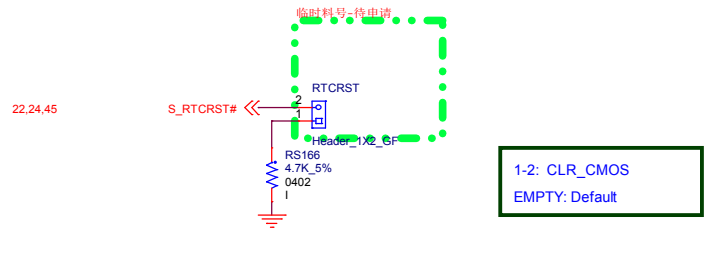
SKU ID



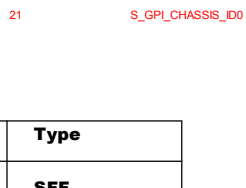
Clear Password



CLR_CMOS



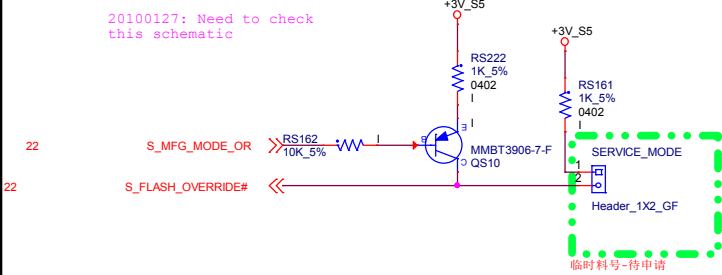
Chassis ID



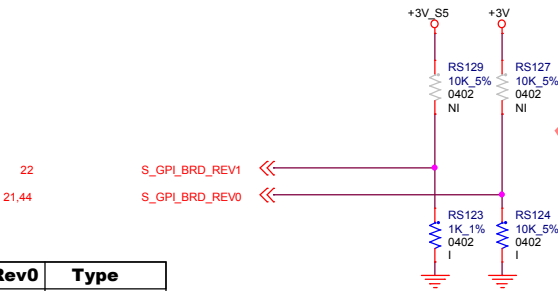
ID0	Type
1	SFF
0	Reserved

Chassis Intruder

ME Disable (Flash override)



BOARD ID



Rev1	Rev0	Type
0	0	Default
0	1	Reserved
1	0	Reserved
1	1	Reserved

Title

PCH-8: MISC CONN/BEEP/ID

DWG NO

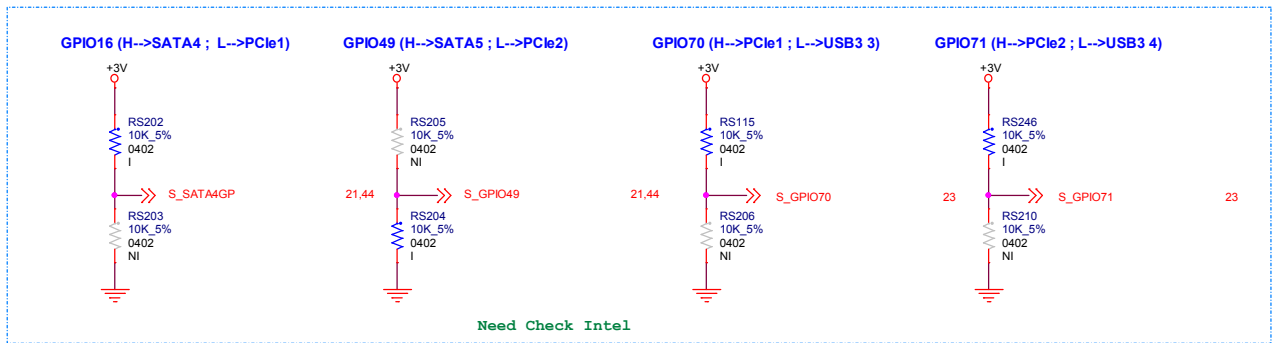
Coral

Rev

X01

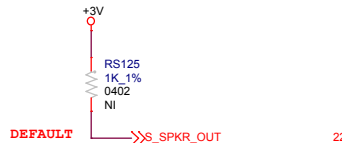
Date: Tuesday, August 12, 2014

Sheet 26 of 91



No Reboot Mode

SPKR (IN-PD)	Description
High	No reboot mode: Enable
Low	No reboot mode: Disable



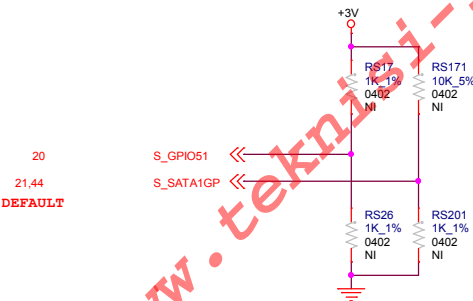
Topblock Swap Mode

GPIO55 (IN-PU)	Description
High	Topblock swap mode: Disable
Low	Topblock swap mode: Enable



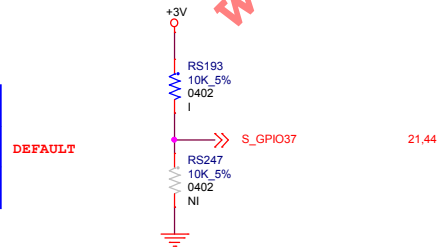
Boot BIOS Destination Selection

GPIO51 (IN-PU)	SATA1GP/GP19 (IN-PU)	Description
Low	Low	Flash cycle routed to LPC
High	Low	Flash cycle routed to PCI
High	High	Flash cycle routed to SPI



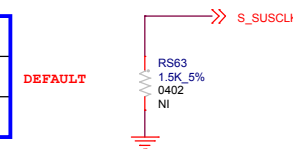
TLS Confidentiality

GPIO37 (IN-PD)	Description
High	ME Crypto TLS cipher suite with confidentiality
Low	ME Crypto TLS cipher suite with no confidentiality



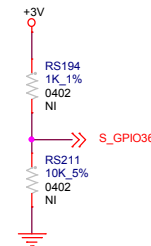
On-Die PLL Voltage Regulator

GPIO62/SUSCLK (IN-PU)	Description
High	Regulator is enabled.
Low	Regulator is disabled.

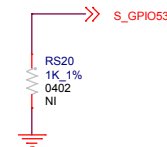


DMI Rx Termination

GPIO36 (IN-PD)	Description
Low	DMI Rx Termination Voltage



DMI AC COUPLING FULL VOLTAGE MODE WHEN SAMPLED LOW



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Title

Block3

DWG NO

Coral

Rev

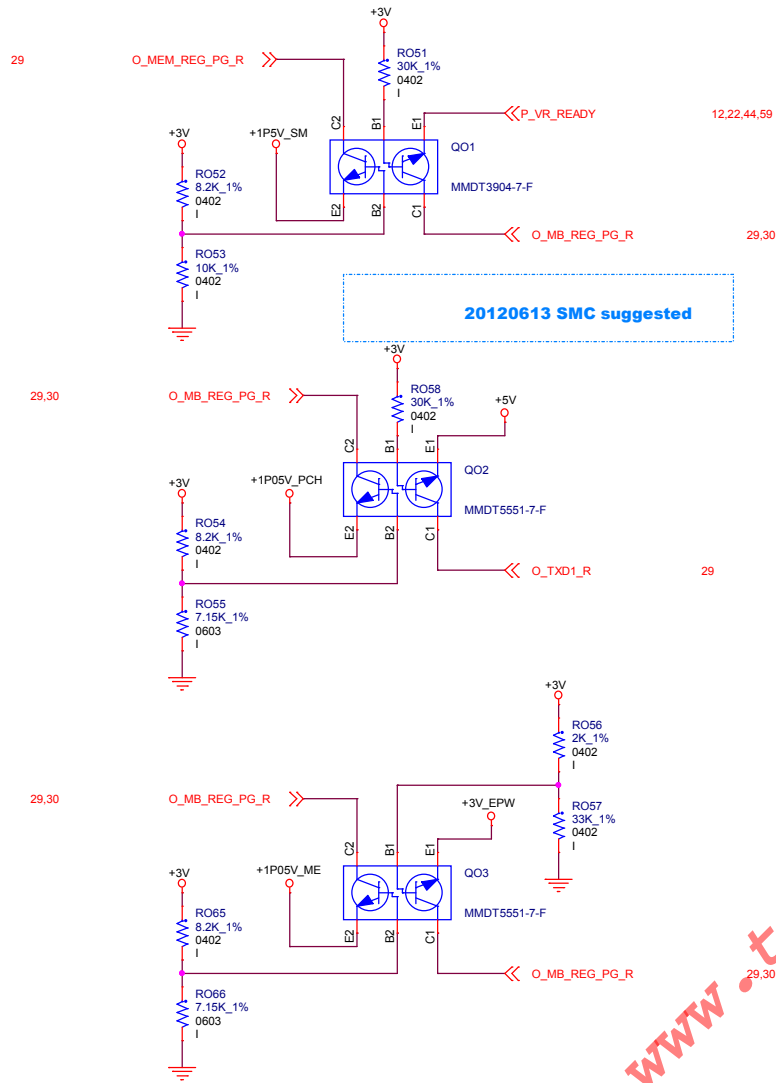
B00

Date: Tuesday, August 12, 2014

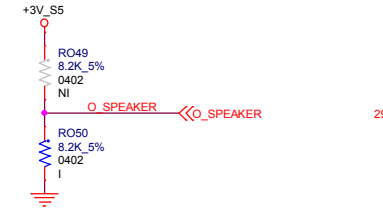
Sheet 28 of 91



5553 PRE-POST DIAG Monitor



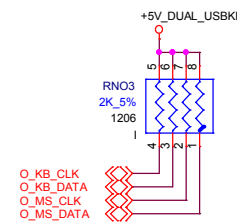
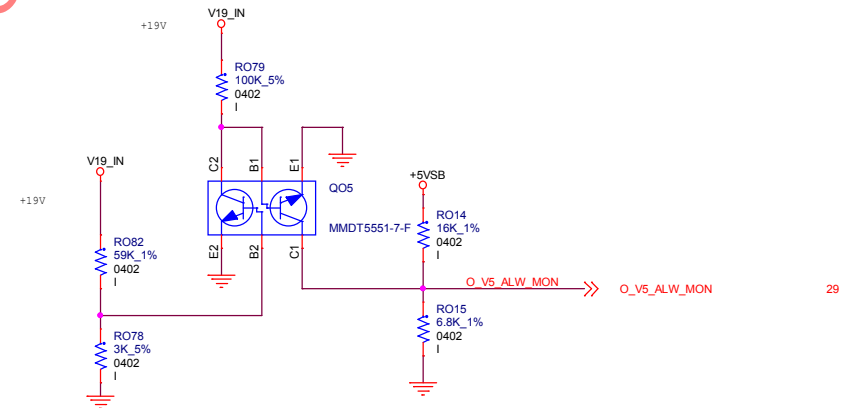
SIO STRAPING

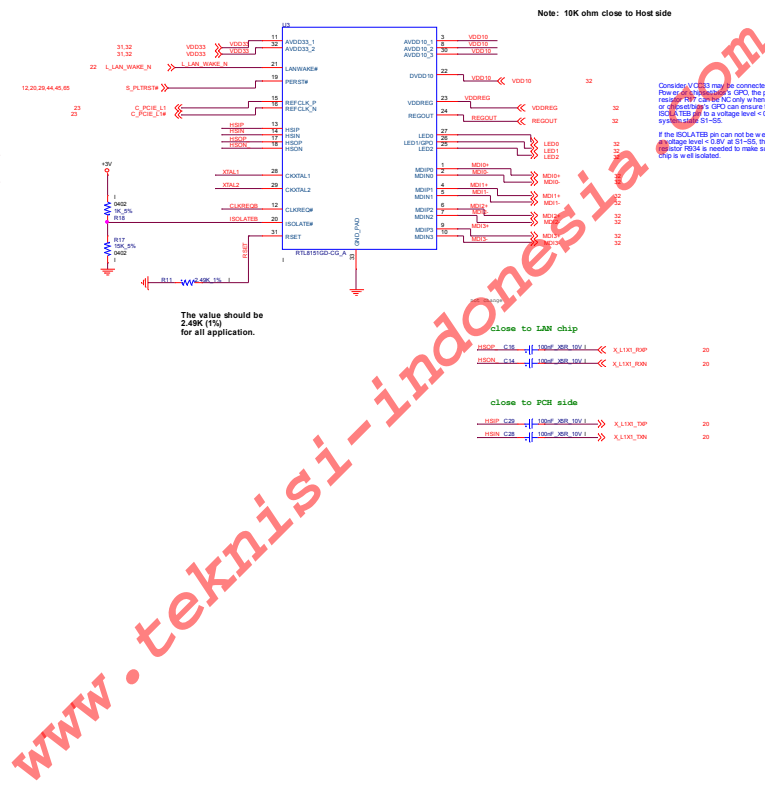


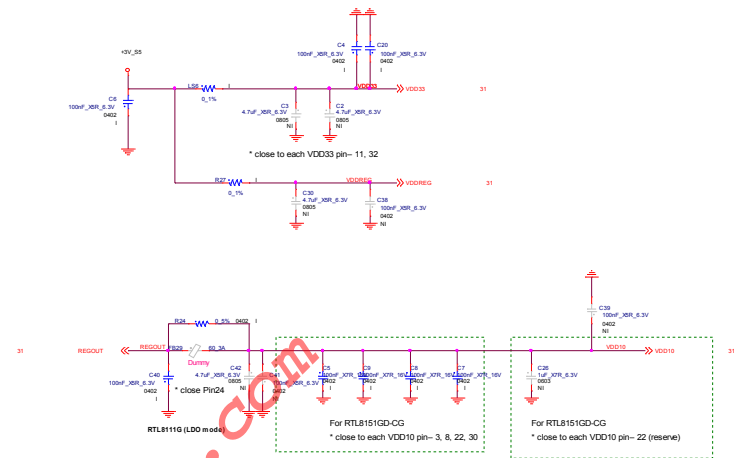
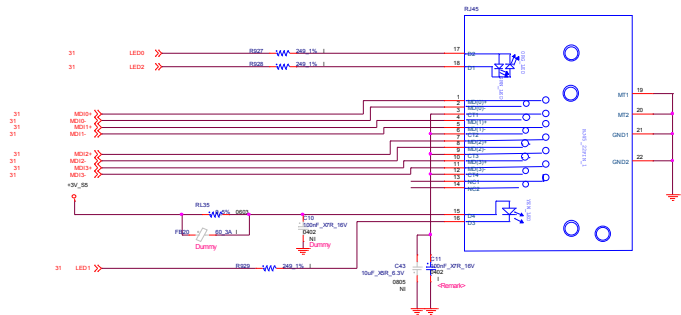
SIO STRAPING

	SPEAKER	
	Diag_En	
PULL HIGH	Disable	
PULL LOW	Enable	

SIO5553 V5_ALW Monitor

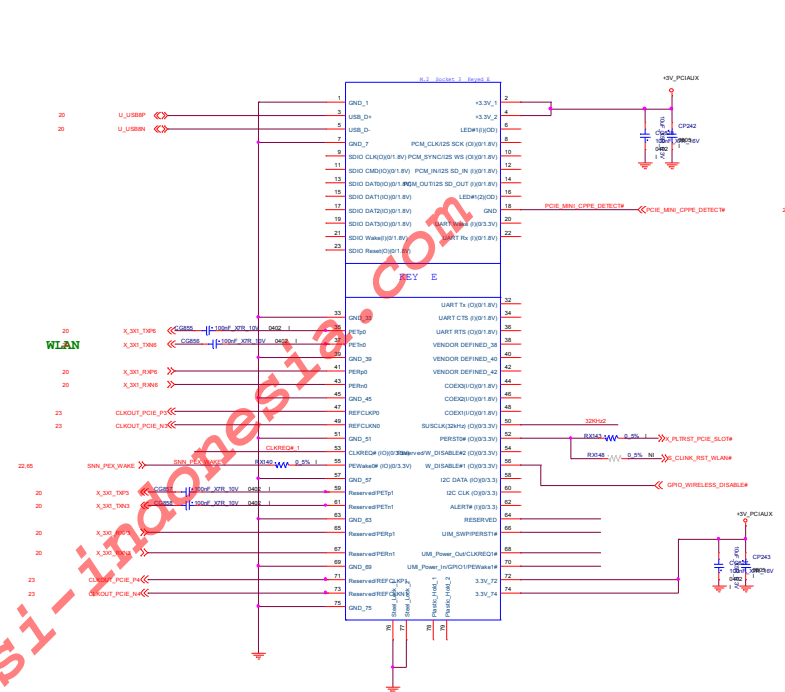
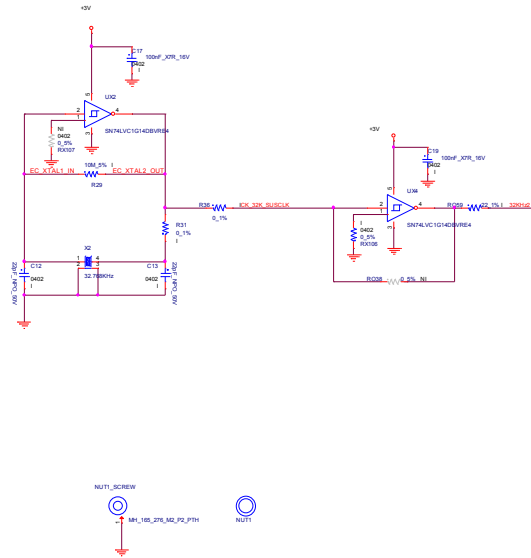


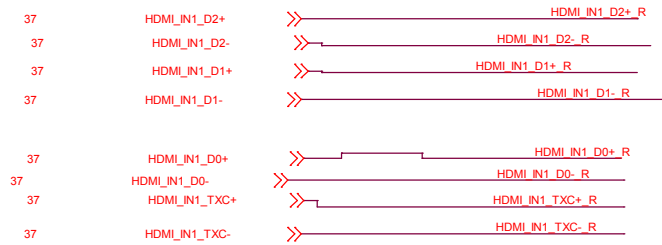
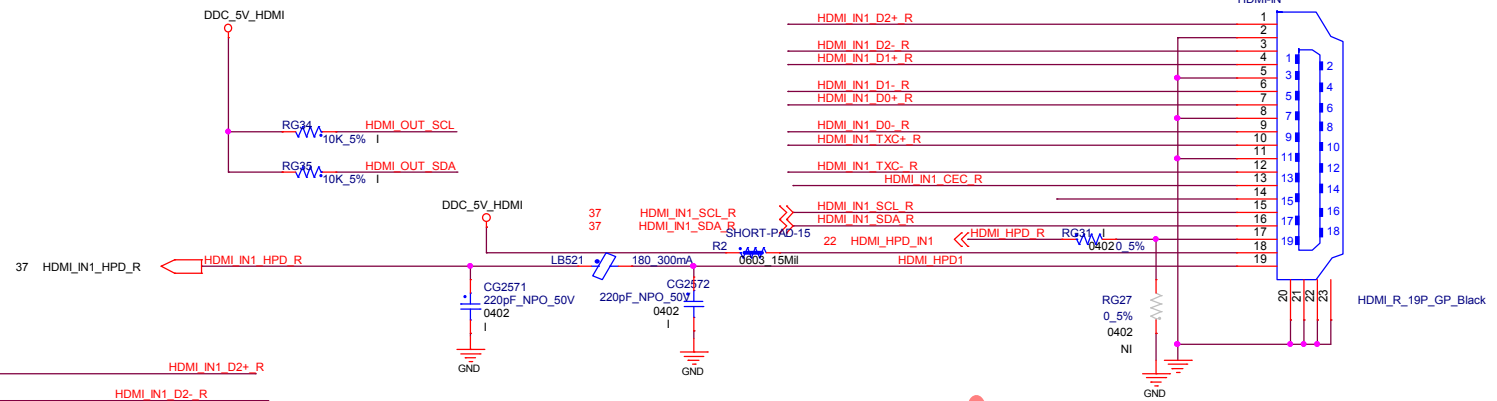
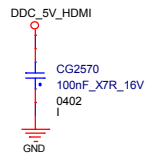




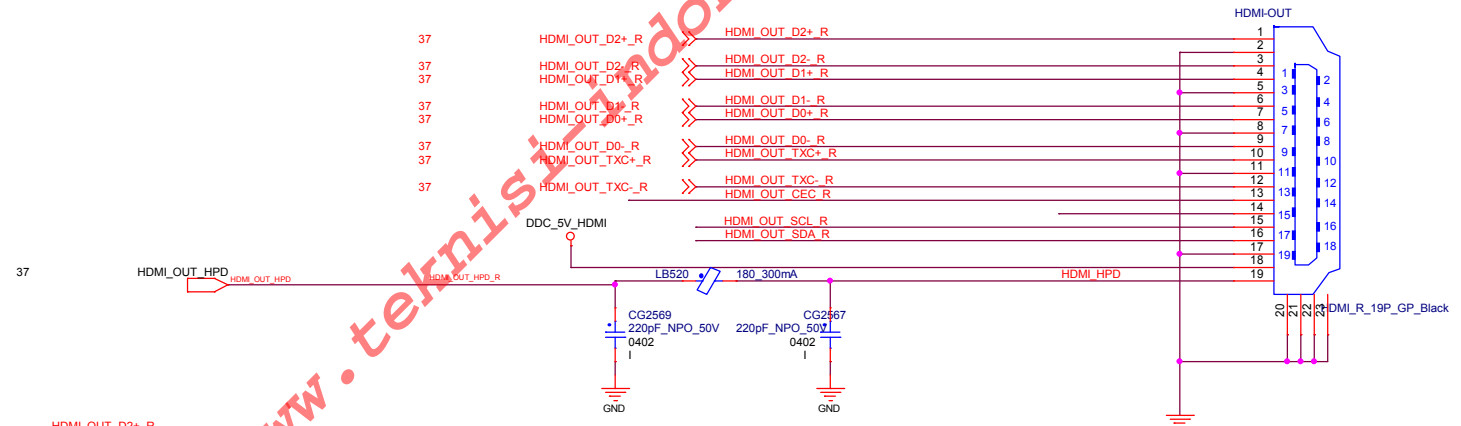
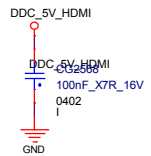
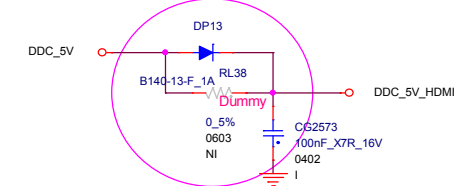
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The diagram illustrates the connection of the XTR25V1 transceiver to the microcontroller. The microcontroller pins CA63 and CA70 are connected to the XTR25V1 inputs through 10kF resistors. The XTR25V1 outputs are connected to the microcontroller pins R210, R211, and R212 through 0.5% resistors. The XTR25V1 is also connected to A_GND.

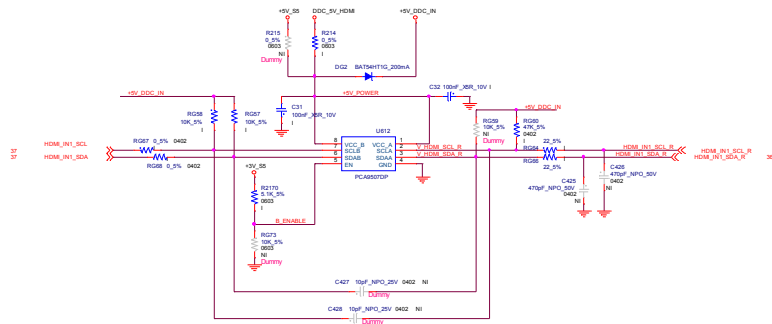




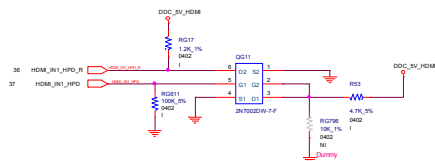
Need to changed



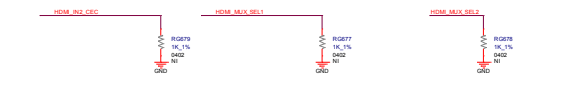
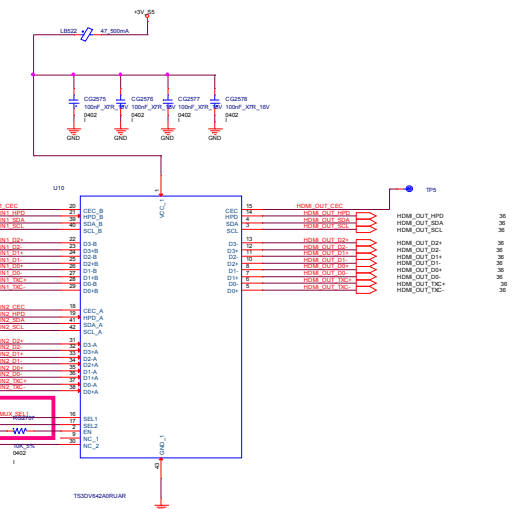
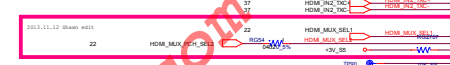
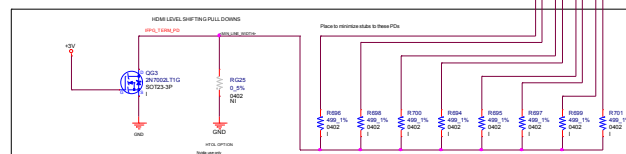
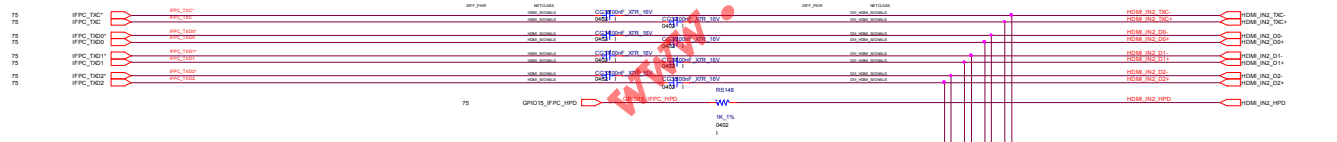
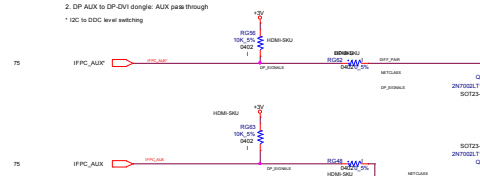
Title HDMI Input/Output Port	
DWG NO Coral	Rev B00
Date: Tuesday, August 12, 2014 Sheet 36 of 91	



C427/C428 and U612 Colay-20140529

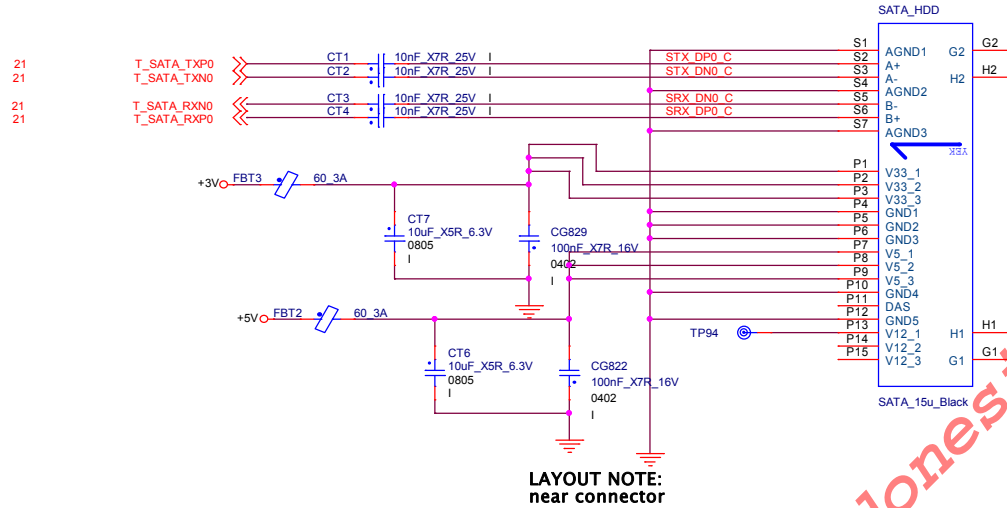


Two cases to be considered:
1. DP_AUX to DP-DVI1 dongle: AUX AC coupled
2. DP_AUX to DP-DVI1 dongle: AUX pass through
* I2C to DDC level switching



HDD SATA CONNECTOR

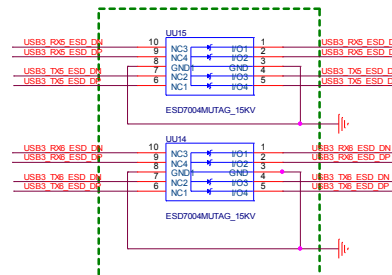
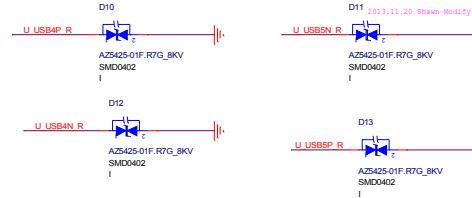
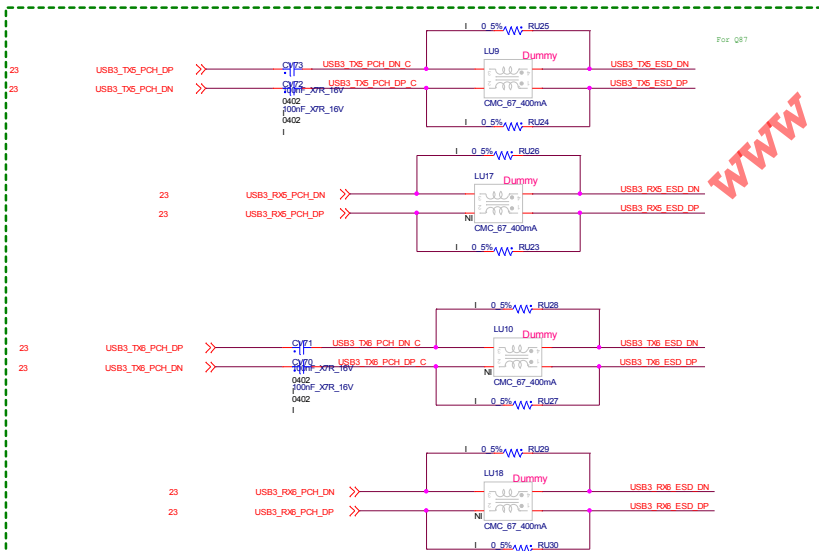
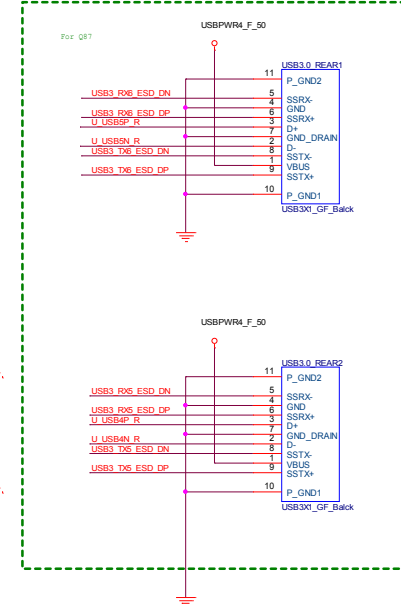
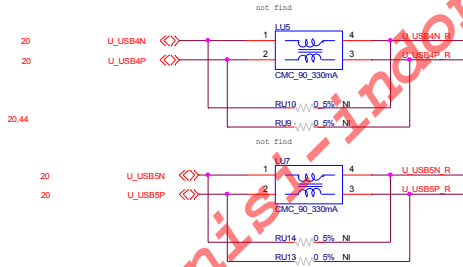
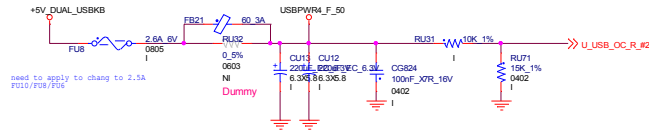
LAYOUT NOTE:
near CONN.



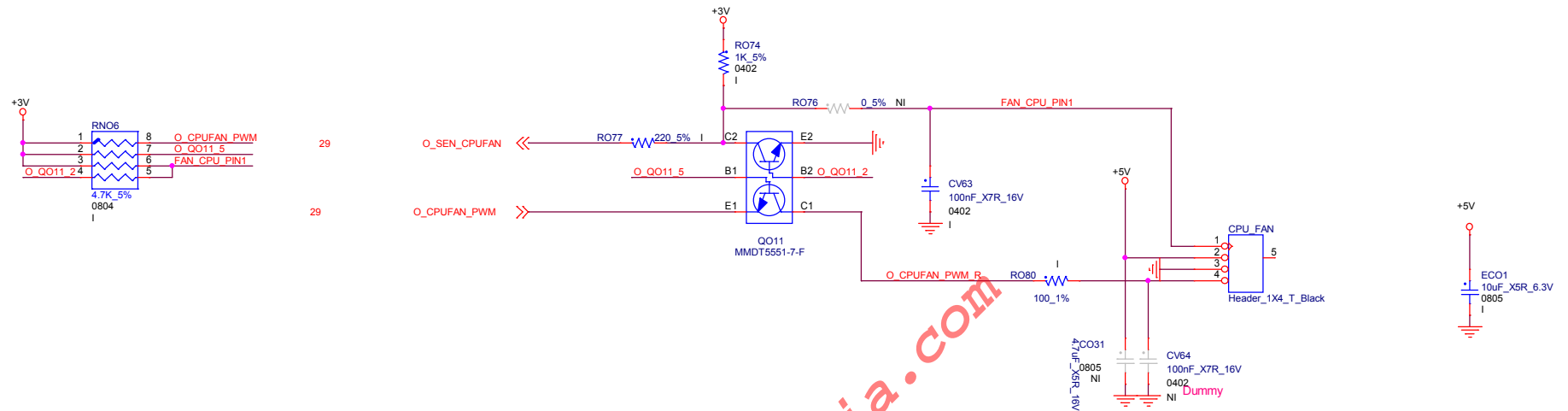
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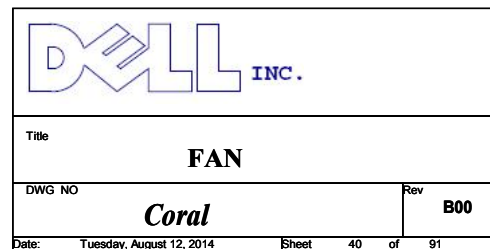
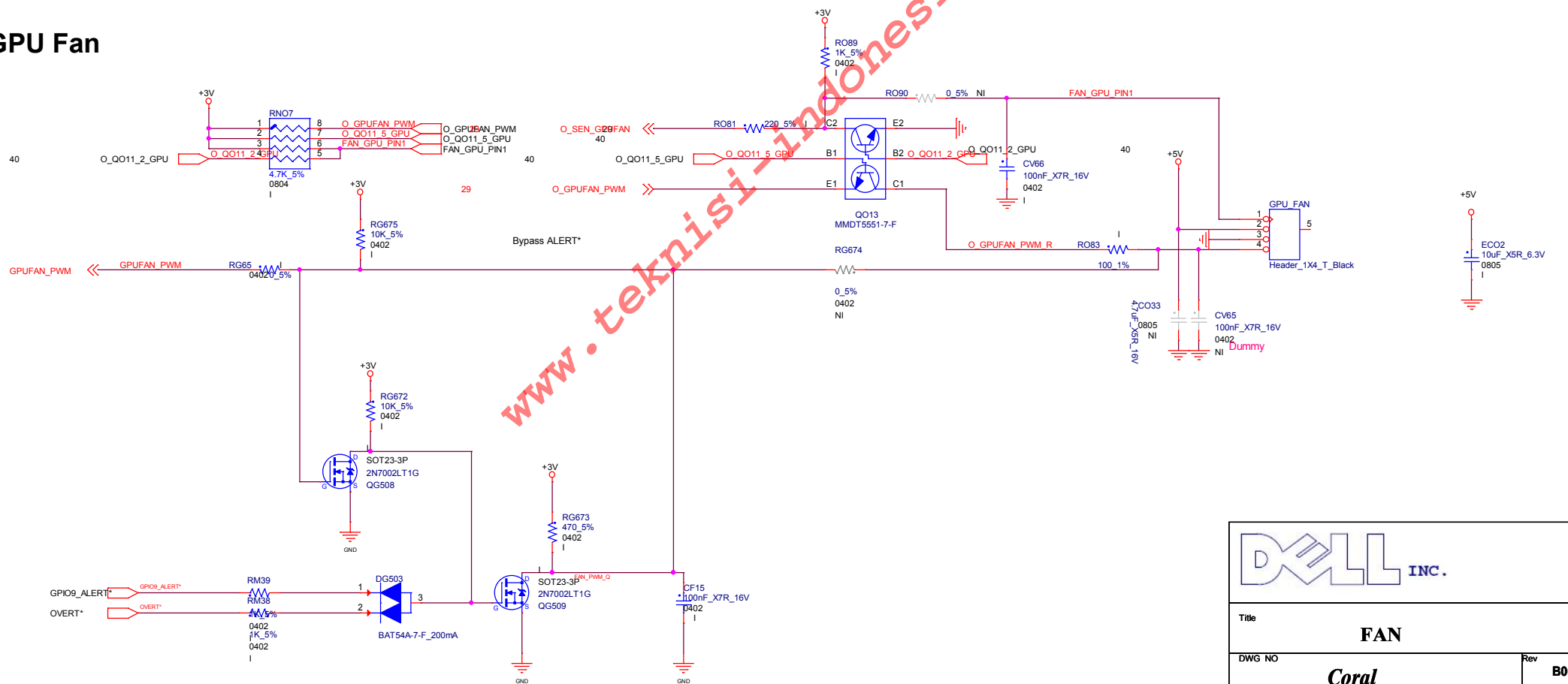
Rear USB 3.0 CONNECTOR

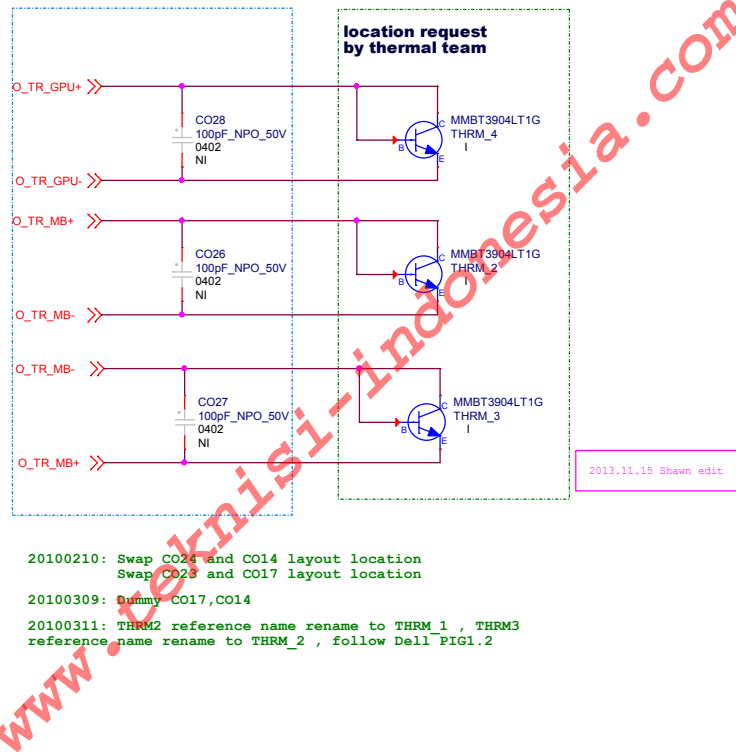


CPU Fan



GPU Fan





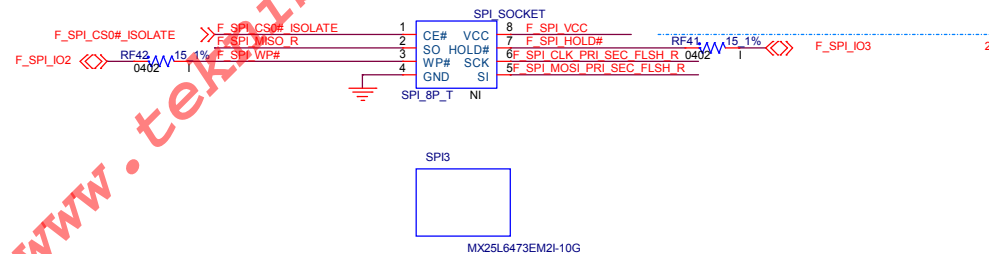
20100210: Swap CO24 and CO14 layout location
Swap CO23 and CO17 layout location
20100309: Dummy CO17,CO14
20100311: THRM2 reference name rename to THRM_1 , THRM3
reference name rename to THRM_2 , follow Dell FIG1.2

2013.11.15 Shawn edit

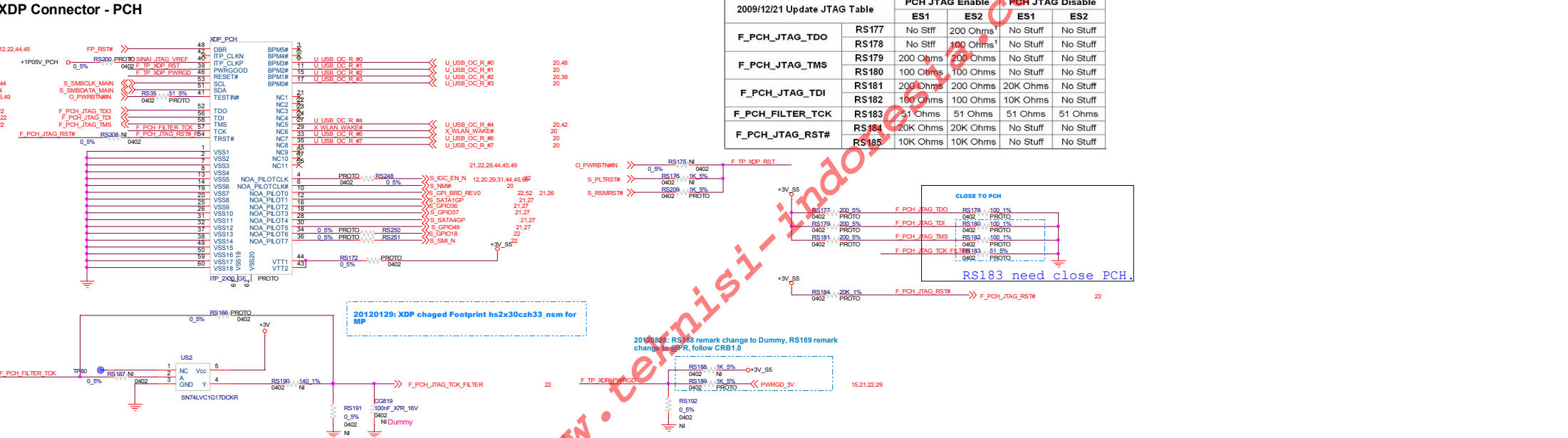
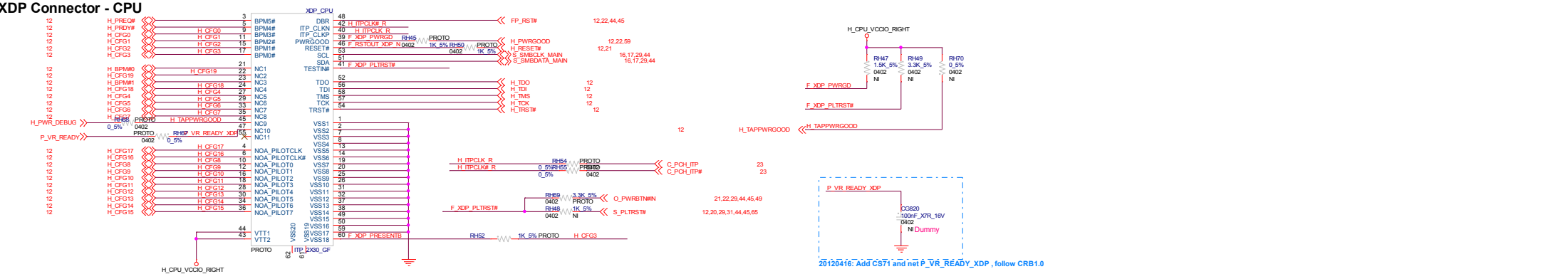


SPI_8MB

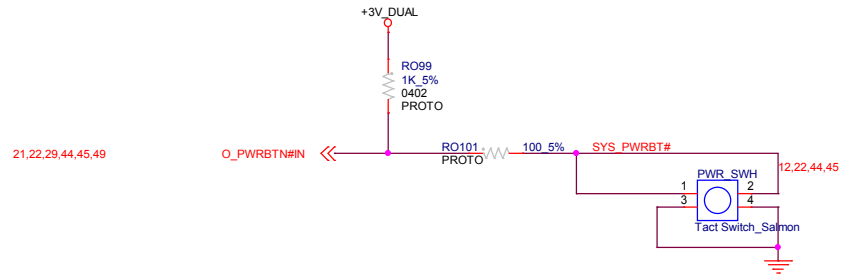
- 20120216: SPI2 rename to SPI3 and Change to 8M , 8 pins flash
20120216: SPI3 and Change to 8M , 8 pins flash, WINBOND_W25Q64FVSSIG
20120917: SPI1 Change to WINBOND_W25Q64FVSSIQ
2012021024: UPDATE VPN



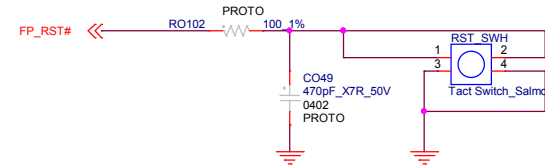
Title SPI	
DWG NO Coral	Rev B00
Date: Tuesday, August 12, 2014 Sheet 43 of 91	



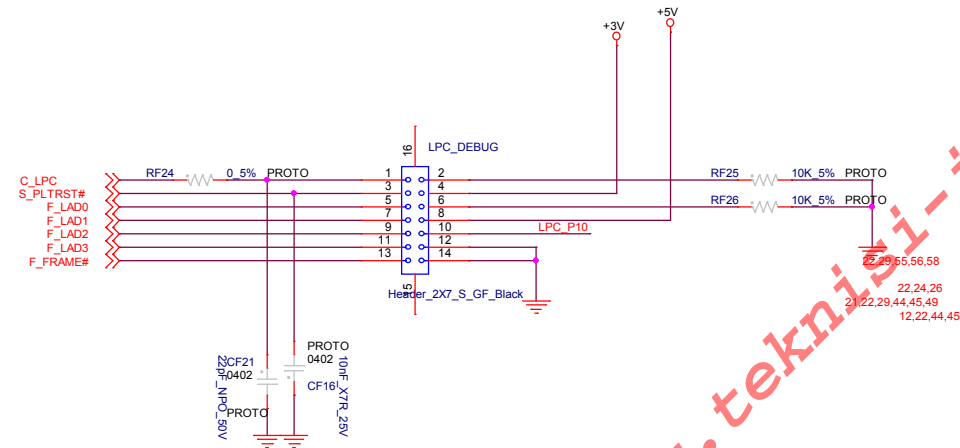
Power Bottom



Reset Bottom

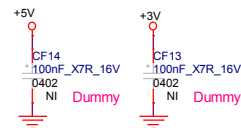
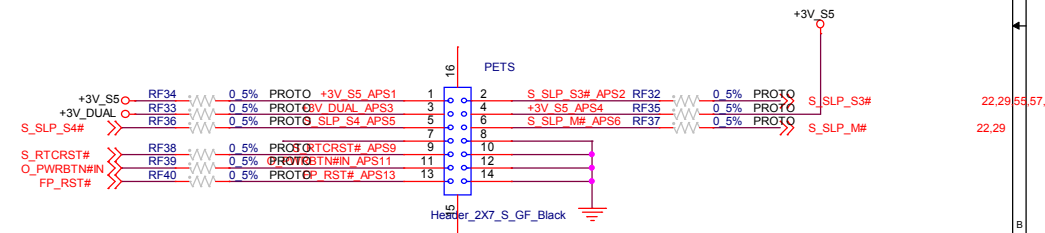


LPC DEBUG




APS Connector

20120627: rename to PETS



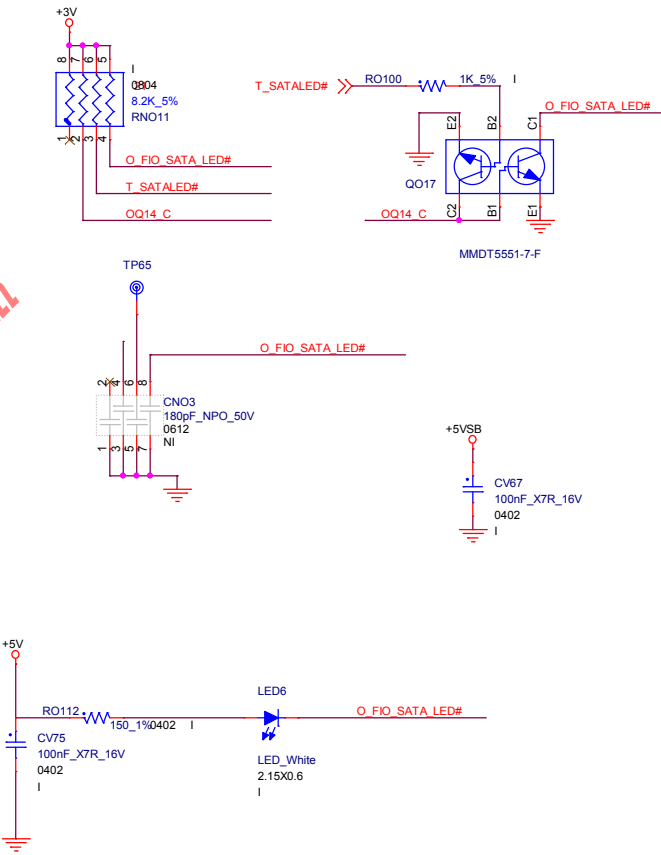
Title		
Pilot Run Conn		
DWG NO	Coral	Rev B00
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Title EMI		
DWG NO Coral	Rev B00	
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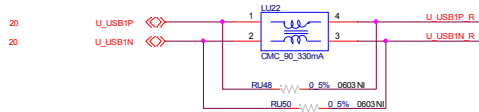
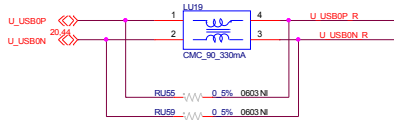
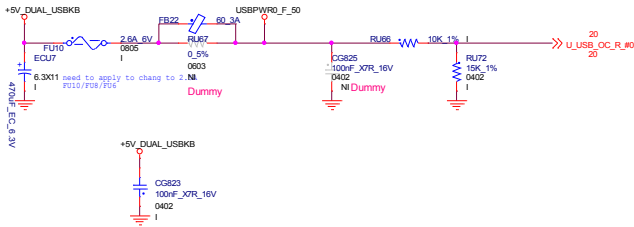
FRONTPANEL Header

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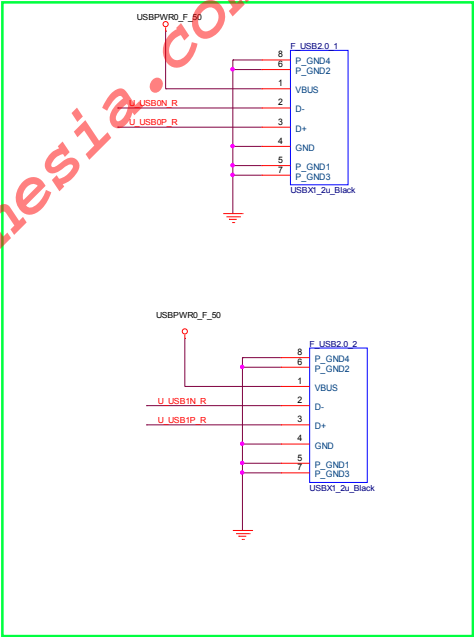
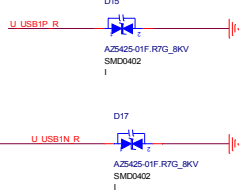
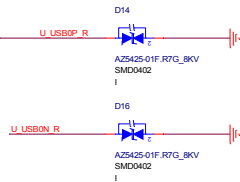


Title		
Front_Panel		
DWG NO	Coral	Rev B00
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Front USB/LED Header

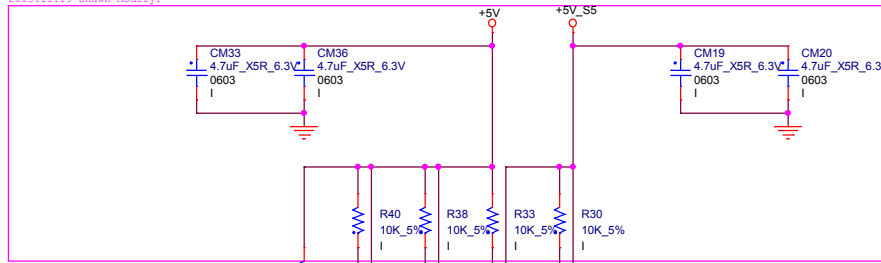


20120309 EMC suggested ESD stuff on FIO board



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2013.11.19 Shawn Modify.

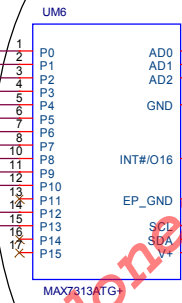


50
50
50
50
50
50
50
50
50
50

EYE_LED_R
EYE_LED_G
EYE_LED_B
RIM_LED_R
RIM_LED_G
RIM_LED_B
LOGO_LED_R
LOGO_LED_G
LOGO_LED_B

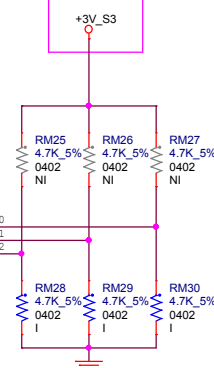
EYE_LED_R
EYE_LED_G
EYE_LED_B
RIM_LED_R
RIM_LED_G
RIM_LED_B
LOGO_LED_R
LOGO_LED_G
LOGO_LED_B

TP91
TP92
TP93
TP59



replace UM6
20131122
Kevin Peng

2013.11.19 Shawn Modify.



2013.11.19 Shawn Modify.

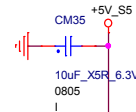
S_SML1_CLK
S_SML1_DATA

S_SMBCLK_RESUME
S_SMBDATA_RESUME

2013.11.19 Shawn Modify.

2013.12.03 Shawn Modify.

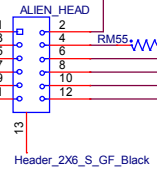
2013.11.19 Shawn Modify.



21

EYE_DETECT
EYE_DETECT

TP61

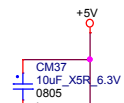


O_PWRBTN#IN

21,22,29,44,45

RIM_LED_R_N
RIM_LED_G_N
RIM_LED_B_N

50
50
50



LOGO_LED_R_N
LOGO_LED_G_N
LOGO_LED_B_N



LOGO_DETECT
LOGO_DETECT

LOGO_LED_R_N
LOGO_LED_G_N
LOGO_LED_B_N

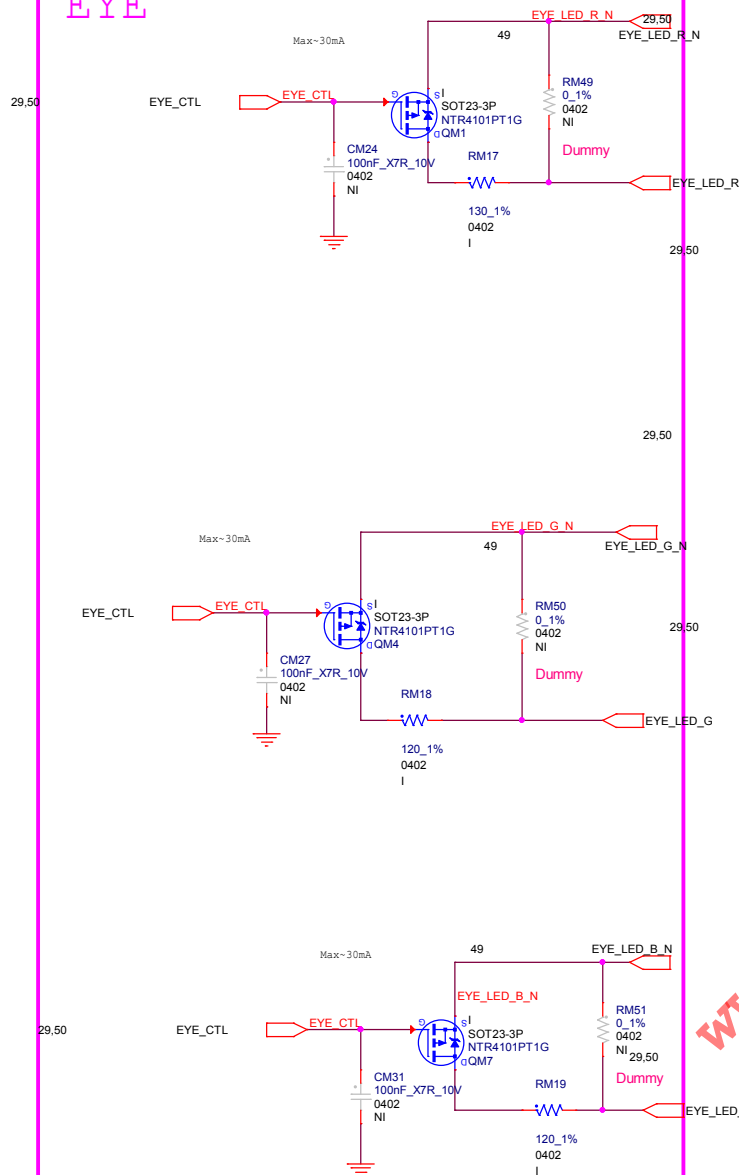
50
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50

Header_2X3_GF_Black

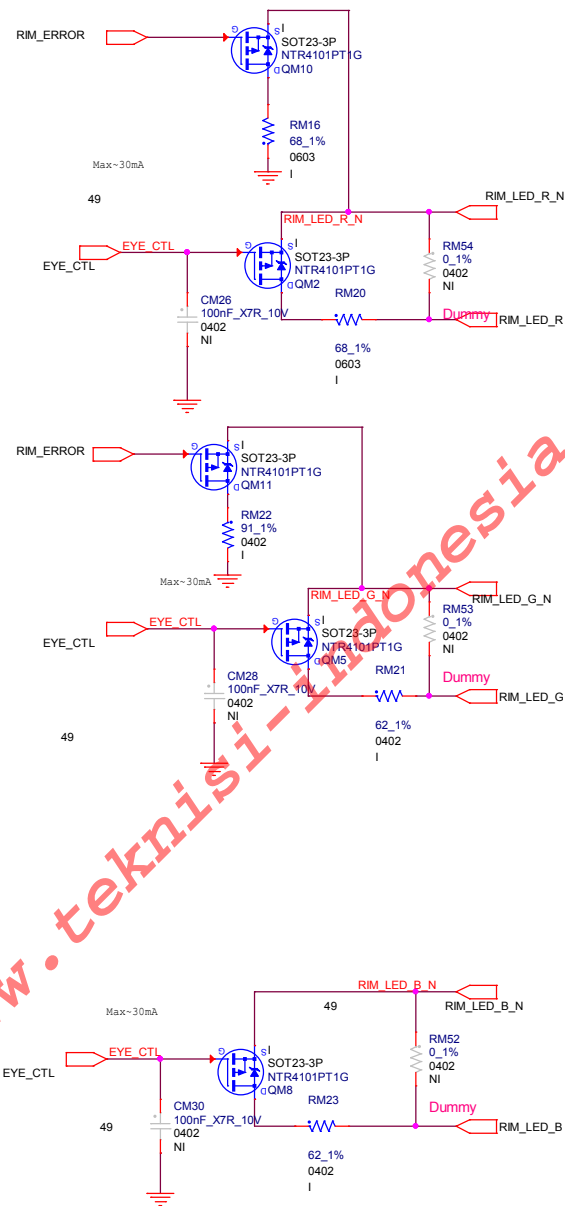


Title	
Alienware LED	
DWG NO	Rev
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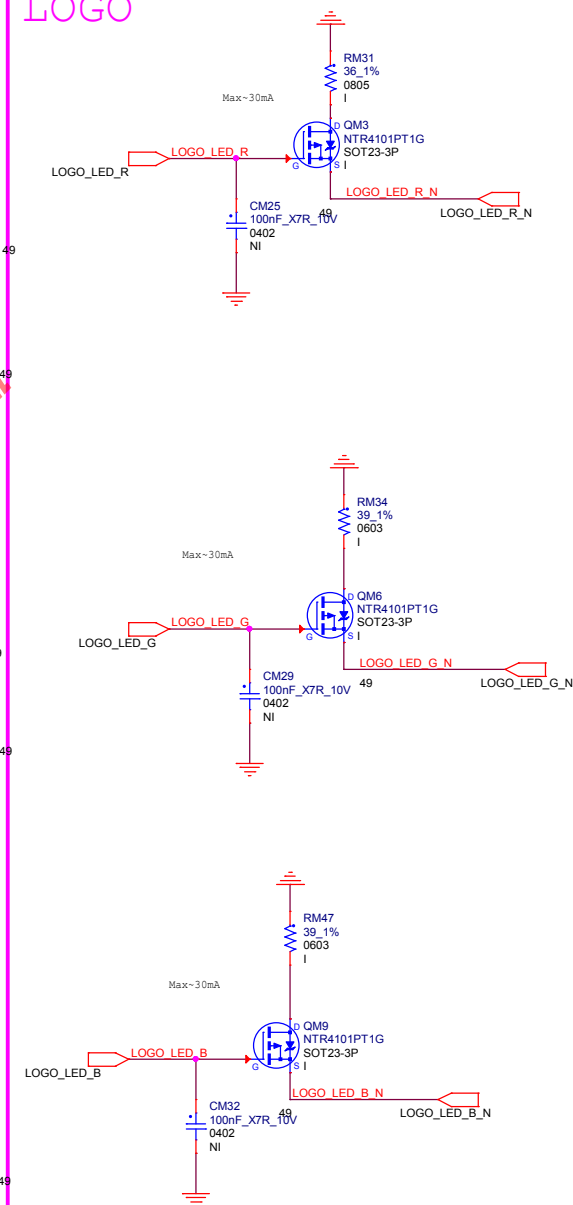
EYE

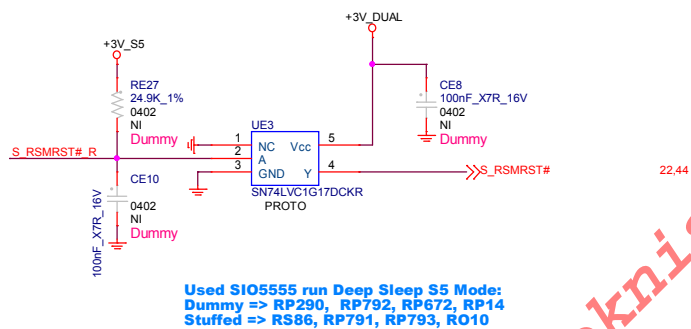
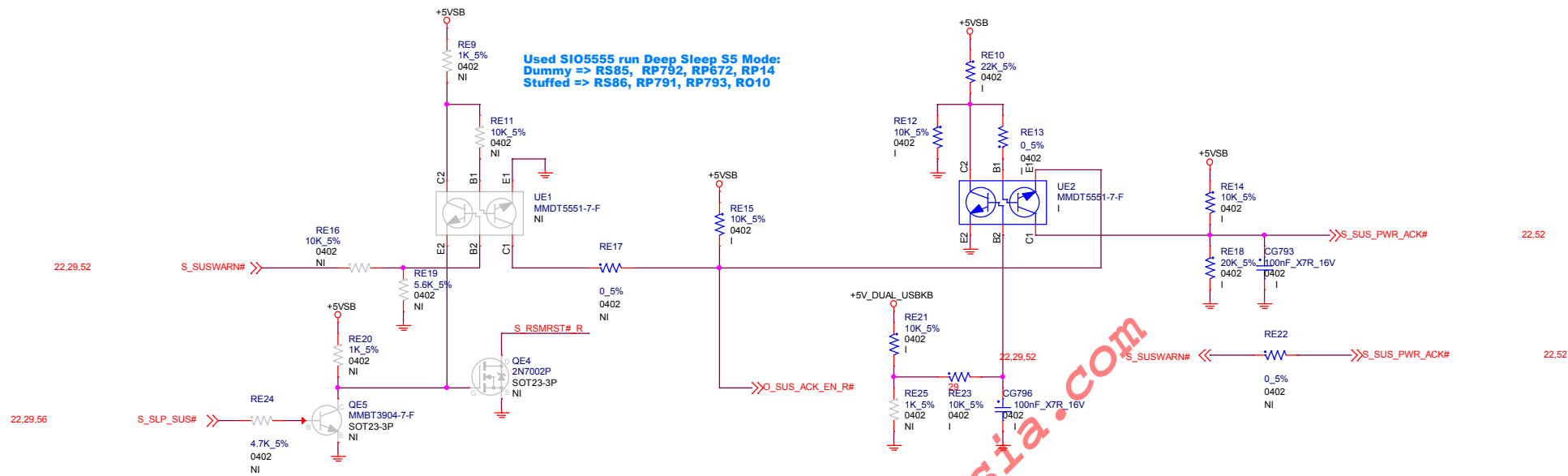


RIM



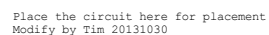
LOGO





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Title Block4	
DWG NO Coral	Rev B00
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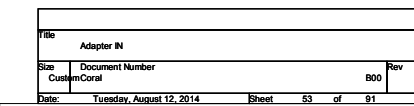


LAN

6V 33.5% >> Adaptor_PSD

ment

23



當Adapter輸出功率超過134W時，OC alert輸出由L變為H。
當Adapter輸出功率由超過134W降至128W以下時，輸出由H變為L。

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

$$T_{on} = 3.85p \times R_{ton} \times V_o / (V_{IN}-0.5)$$

$$f = V_o / (V_{IN} \times T_{on}) = (V_{IN}-0.5) / (3.85p \times R_{ton} \times V_{in})$$

$$= 337.2K \text{ Hz}$$

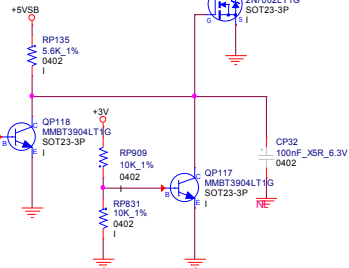
need check
20131122

+VDDQ_VTT Iout=1A
+1P5V_SM_VTT

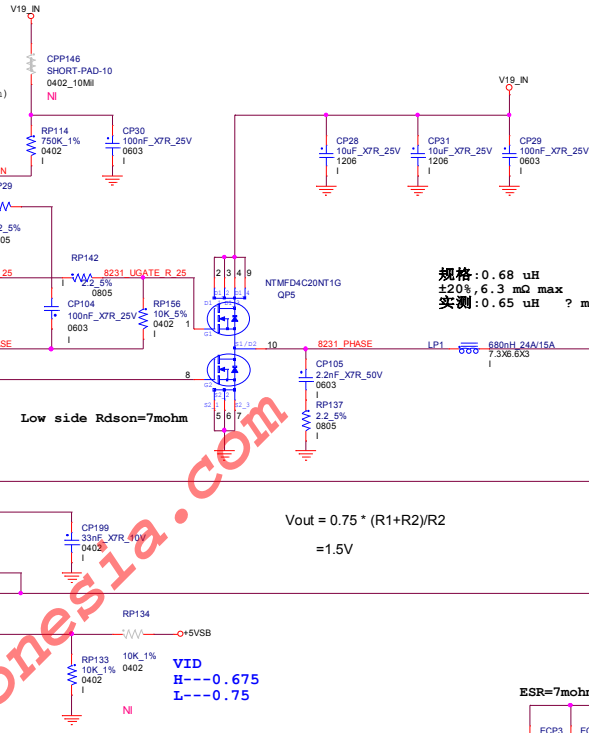
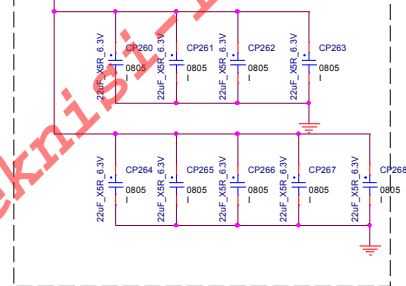
OCP
 $R_{lim} = (I_{lim} \times R_{dson}) \times 10 / 5uA$

For S3 Pin& S5 Pin setting

V SM ENABLE CIRCUIT



PLACE ALL 0805 CAPS INSIDE
CPU SOCKET CAVITY



+1P5V_SM=1.5V
Iout=12A
OCP=20A

规格: 0.68 uH
±20%, 6.3 mQ max
实测: 0.65 uH ? mQ

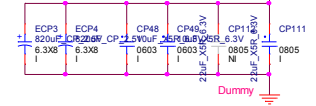
Low side R_{dson}=7mohm

$$V_{out} = 0.75 \times (R_1 + R_2) / R_2$$

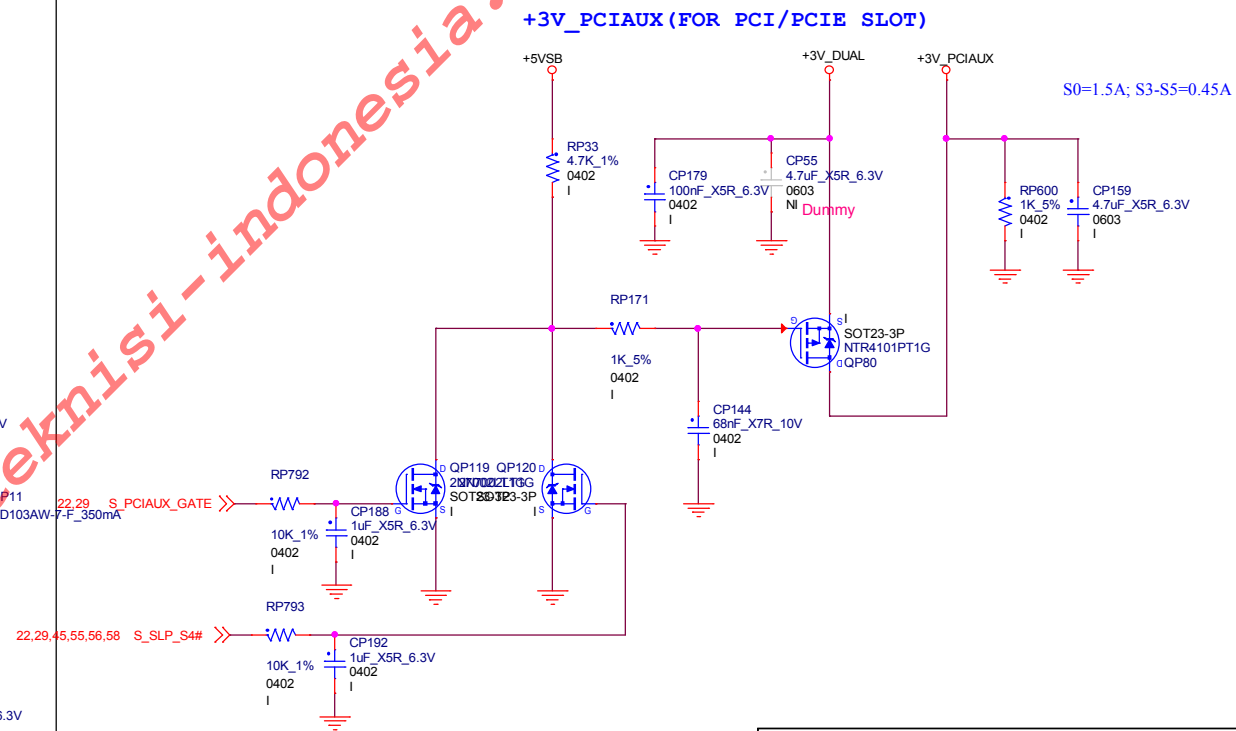
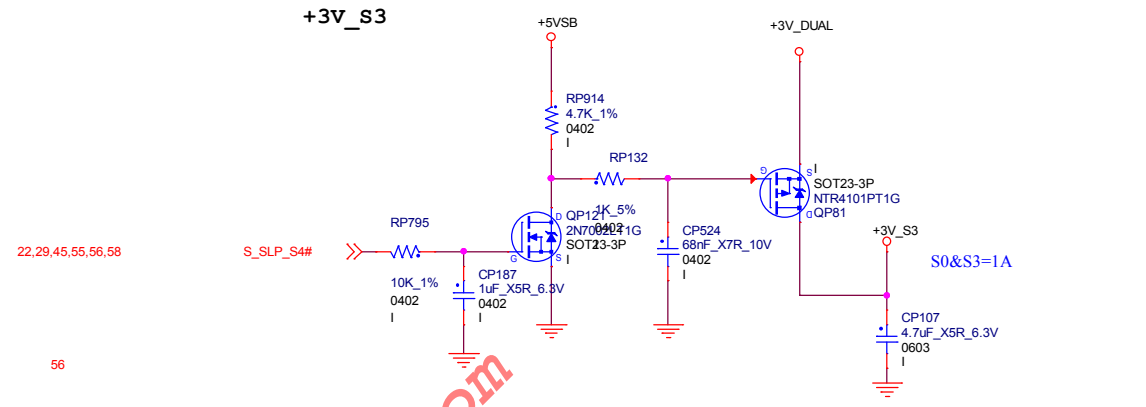
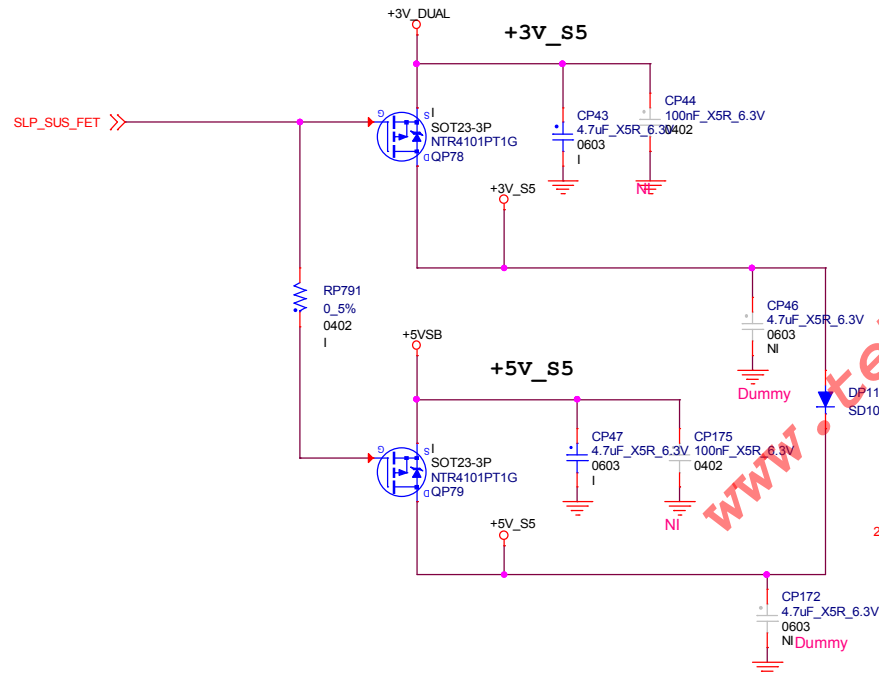
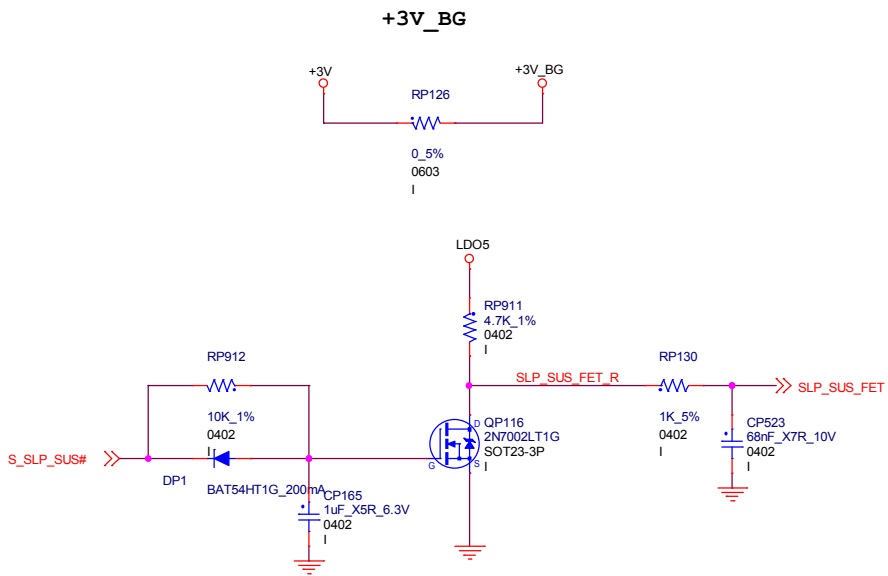
$$= 1.5V$$

VID
H---0.675
L---0.75

ESR=7mohm

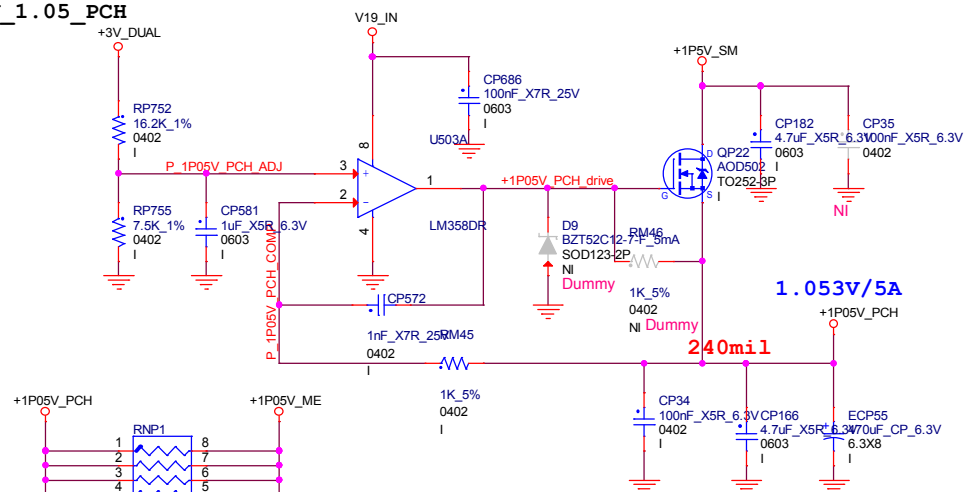


Title	VR_MEM/VTT	Rev	800
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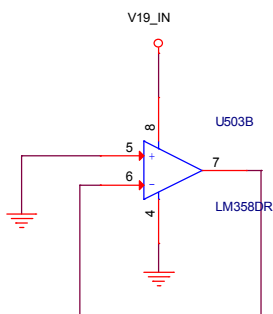
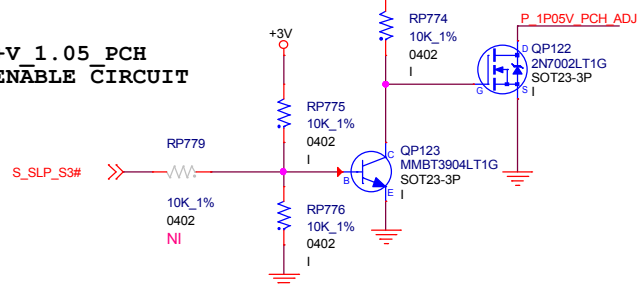


Title		
5V_S5/3V_S5/3V_PCIAUX		
Size	Document Number	Rev
B	Coral	B00
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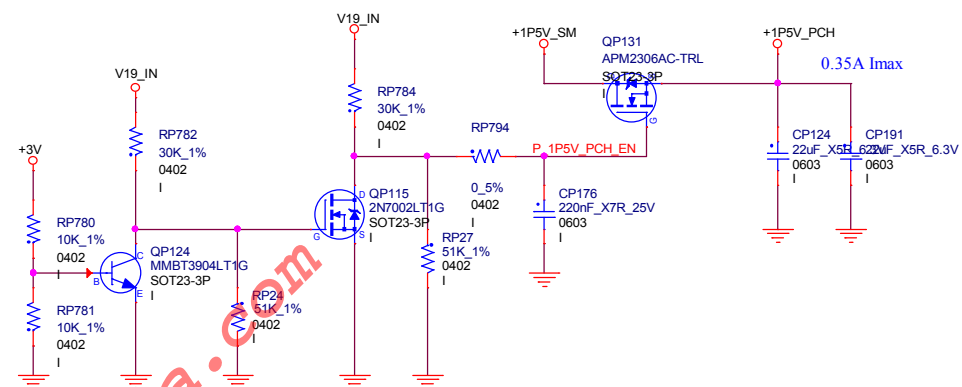
+V_1.05_PCH



+V_1.05_PCH ENABLE CIRCUIT

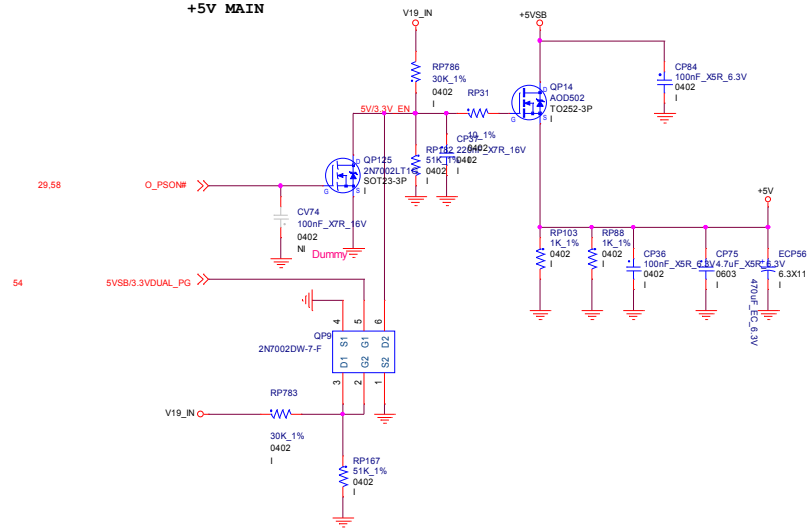


+V_1P5_PCH

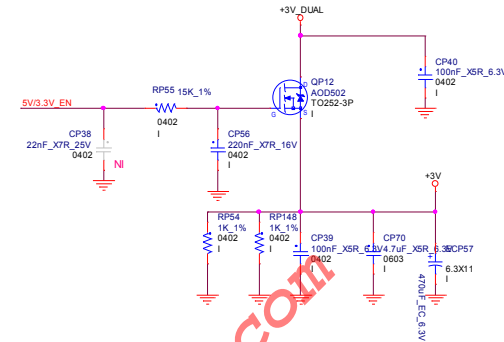


Title			
1.05V_PCH/1.5V_PCH			
Size	Document Number	B00	Rev
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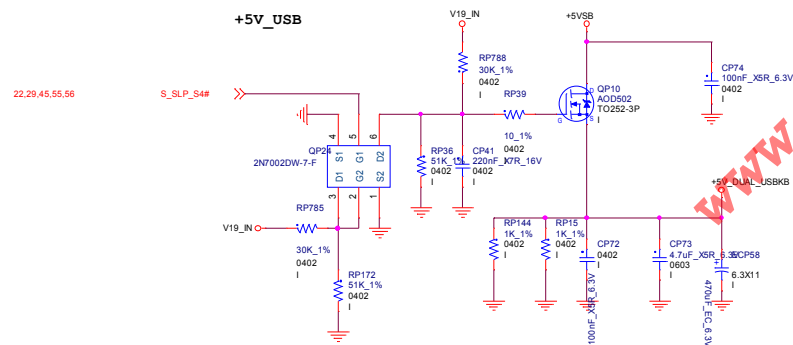
+5V MAIN



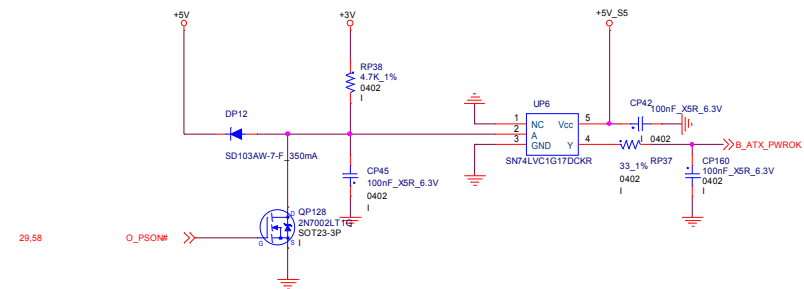
+3V MAIN



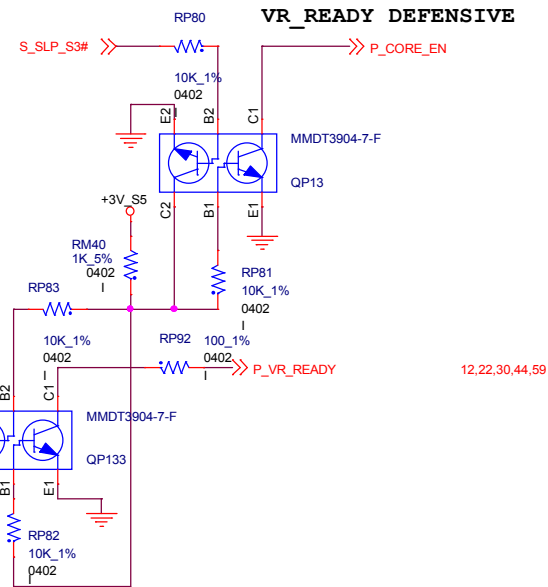
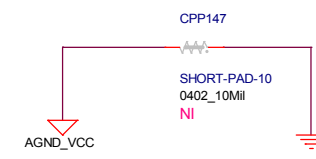
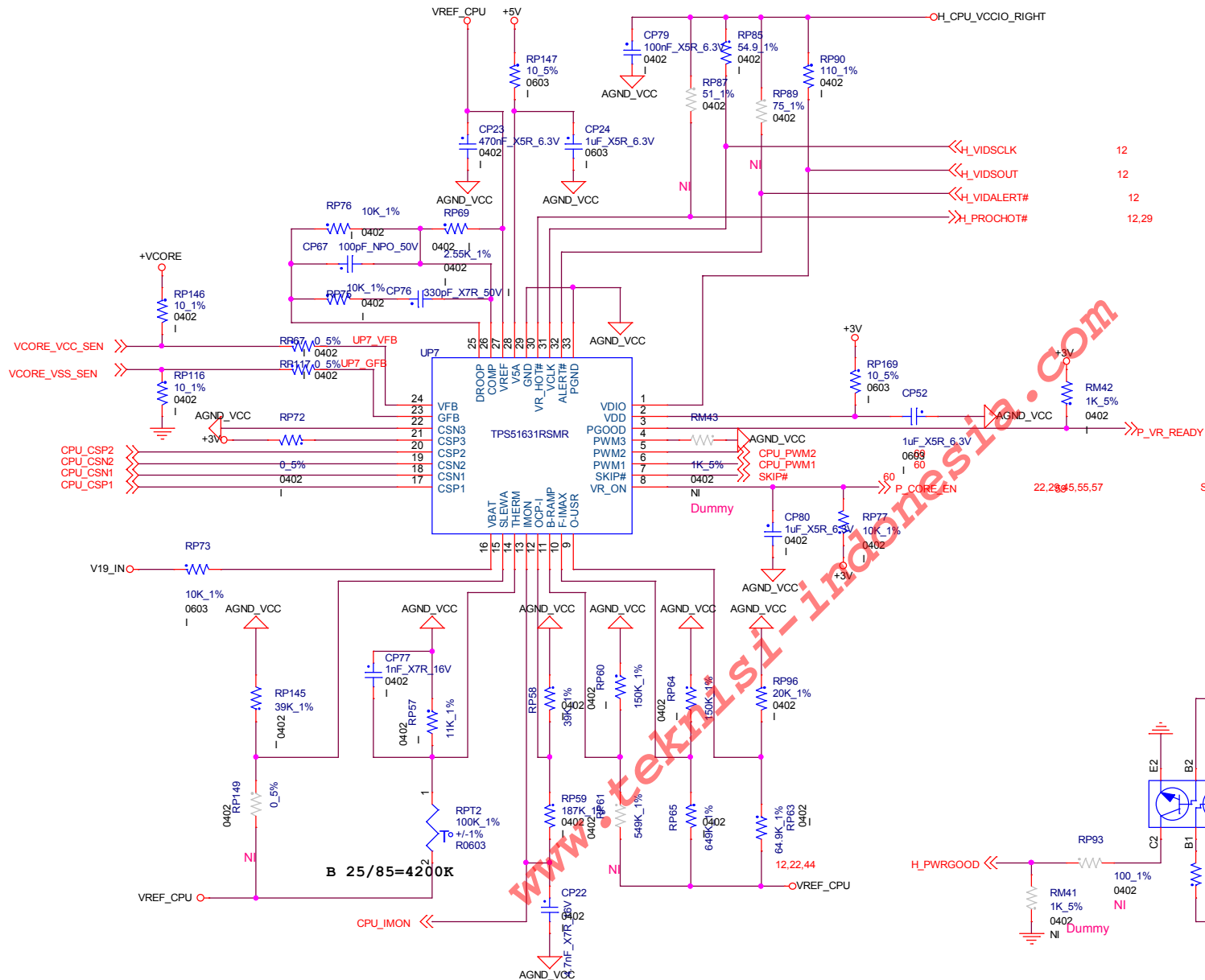
+5V_USB



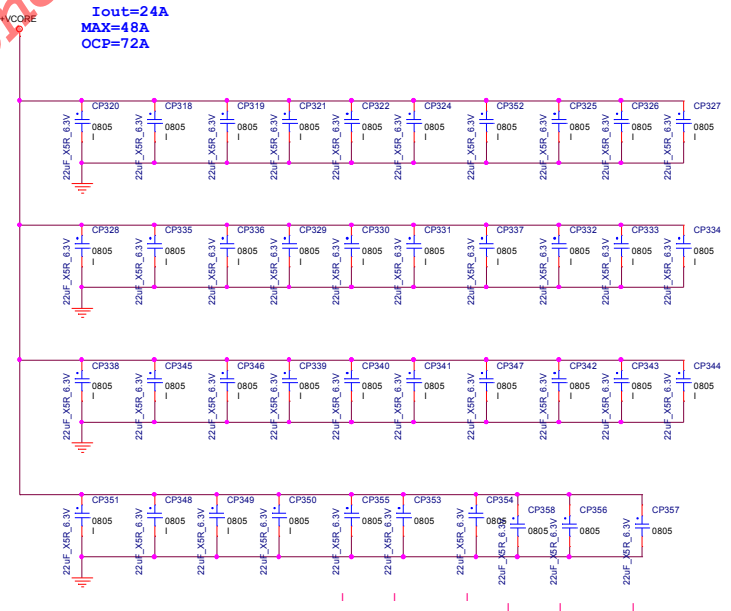
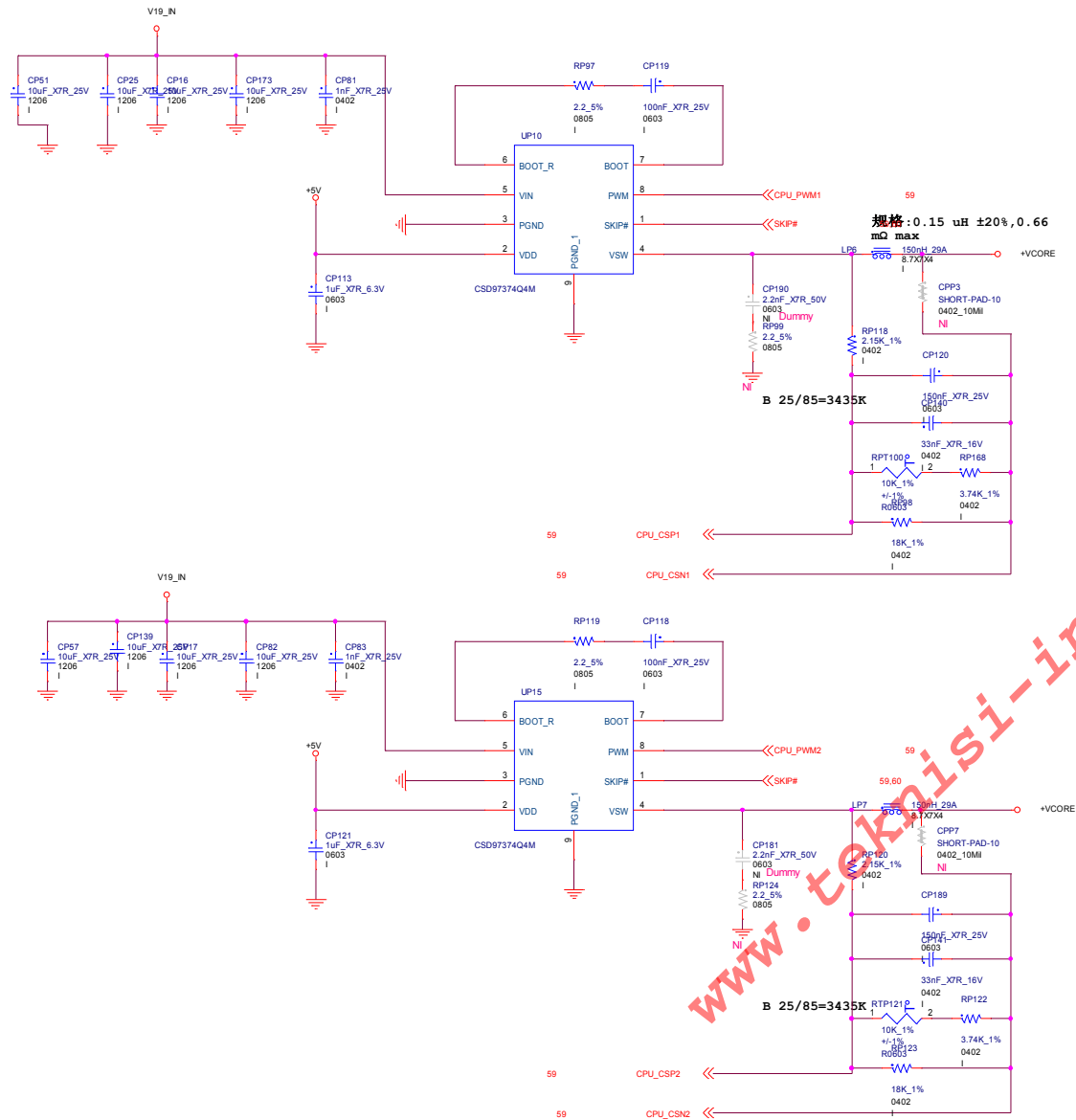
New ATX_PWR0K



60
60
60
60



Title			Vcore PWM
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2.RJ45 TBD need to update footprint---ok

4. LPC and APS need to be update to SMD--ok

9. CPU FAN--ok

6. SATA-HDD need to add footprint---ok

10. DP and APS--OK

12. LU19,LU22 PAGE51---OK

13. lp5,lp6,lp12,lp15 net in fail. Remove--OK

14. USB comm CHOCK---OK

15. DA4/DA5/DA6/DA7 TBD PN--OK

15. FV2/FV3/FV1 for layout footprint issue --OK

7. Need add tow standoffs for M2 connector and add TBD PN--ok

11. QV12,QV15,QV17,...QV20 for VGA----OK

1.UF3 need to be updated page 44

8. Need add footprint for tow audio jacks

16. Battery connector

17. PSW/RTC/Server mode header

18. Intruder switch

3. DIMM2 update HHPN

5. UH1_1 symblo need to add footprint

0924 下午 for 0.7 BOM
1.update SO-DIMM PN
DIMM1: from AS0A626-H2S6-7H to AS0A62E-H2SB-7H
DIMM2: from AS0A621-HASN-7H to AS0A62E-HASB-7H
2.SERVICE_MODE/RTCRST/PSWD change from 340600L00-600-G to 34067AW00-600-G
3.SPI3 8MB ROM change from 41050RK00-205-H(winbond) to 41050SR00-233-G (MXIC) Dell 禁用winbond

Title		
Change list		
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E2704-A00

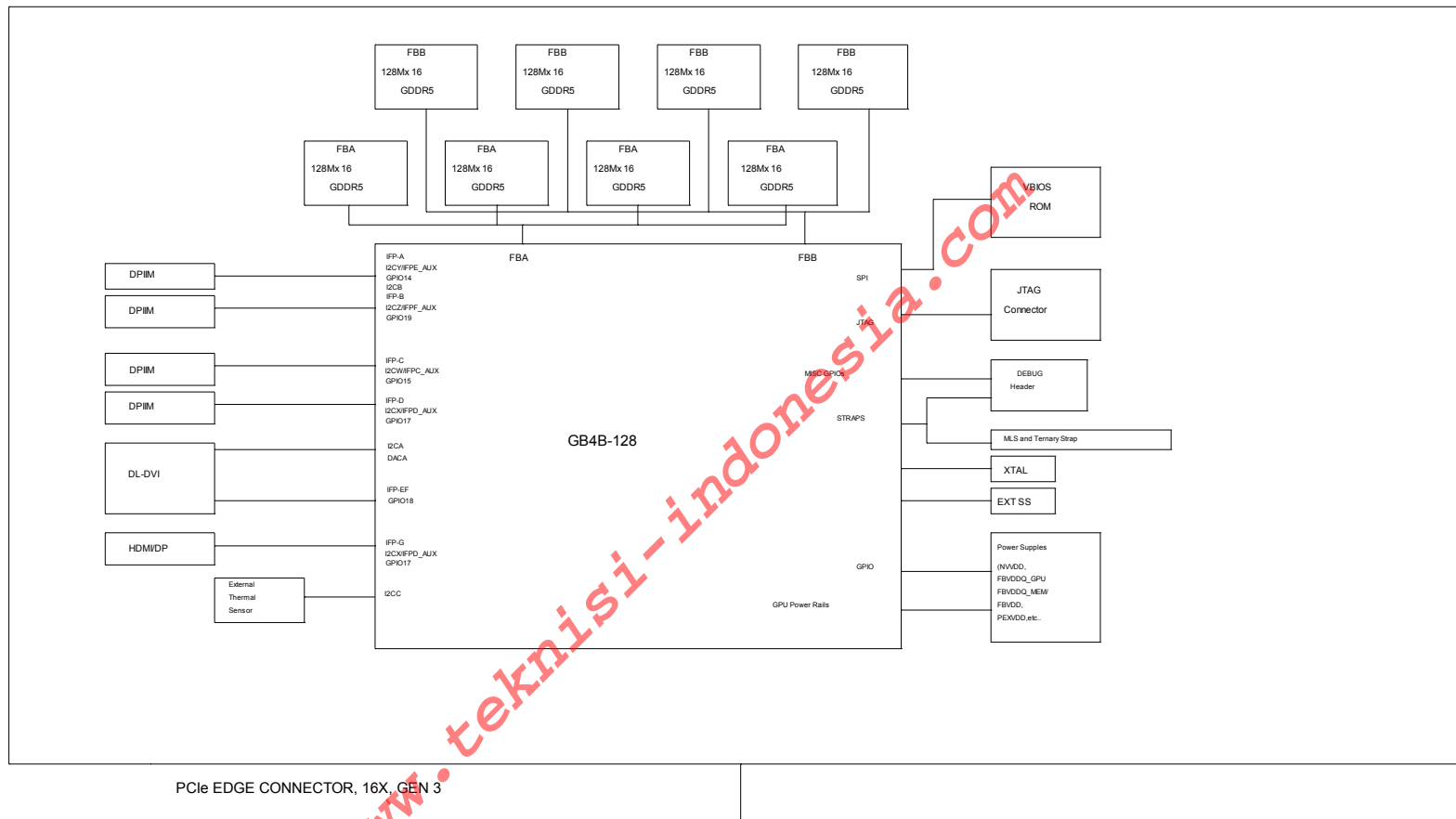
GM107/GM108/GK107/GK208/GF117 GDDR5 NOTEBOOK REFERENCE BOARD
LVDS,2xDPIIM,HDMI/DP and DL DVI-I

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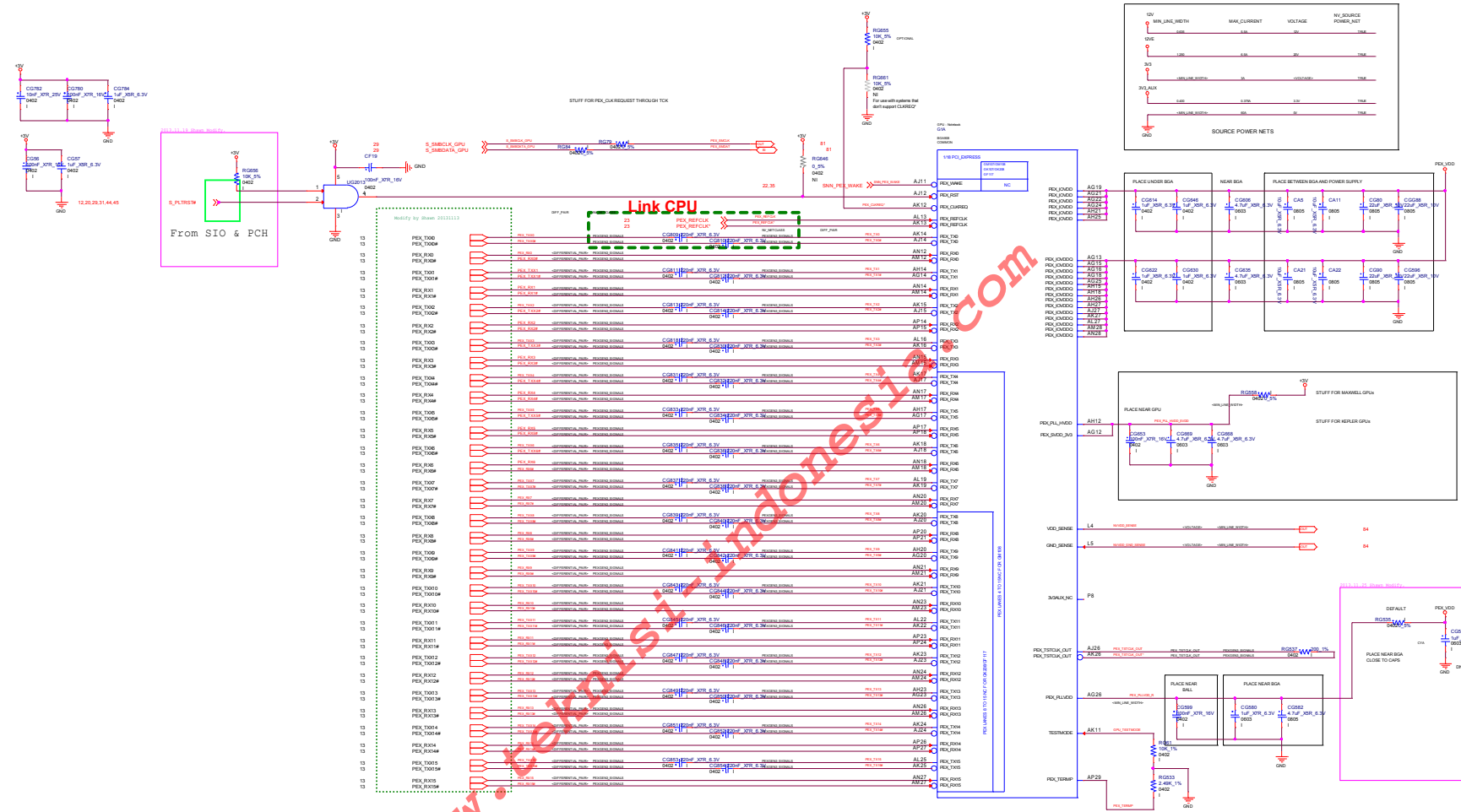
Page	Description
1	Table of Contents
2	Block Diagram
3	PCI-Express Gen3 x16 Interface
4	Frame Buffer Partition A
5	Frame Buffer Partition A - Lower Half
6	Frame Buffer Partition A - Upper Half
7	Frame Buffer Partition B
8	Frame Buffer Partition B - Lower Half
9	Frame Buffer Partition B - Upper Half
10	FBVDDQ Decoupling Caps
11	NVVD Decoupling Caps
12	IFPA/B 2xDPIIM
13	IFPC DPIIM
14	IFPD DPIIM
15	IFPEF DL-DVI
16	IFPG HDMI/DP
17	DACA
18	VB IOS ROM,XTAL, External SS and 3V3_AON/VDD33
19	GPIOs, Thermal Sensor, I2C Repeater
20	Status LEDs
21	JTAG, Fan Control, Auxiliary Devices
22	Straps
23	NVVD OVR2+1
24	NVVD EDP Measurement
25	FBVDD/Q

Page	Description
26	5V_SW/3V3_SW,3V3 LDO
27	Miscellaneous Voltage Rails
28	PEX_VDD Switcher
29	Power Supervision and Sequencing Controller
30	Power Enables-1
31	Power Enables-2 and FBVDDQ_AON
32	Remote Voltage/Current Sensing
33	Input Power Select Circuit and Input Power Measurement
34	Panel Power Remote Sense
35	Discharge Circuits
36	Mechanical Components

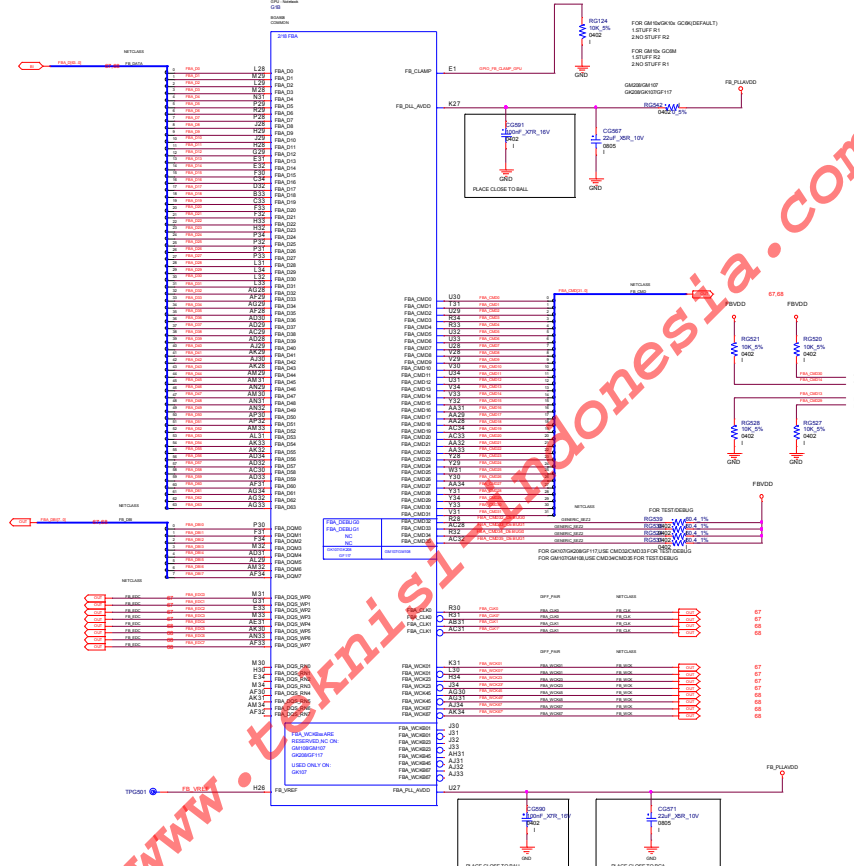
2. Block Diagram



3. PCI-Express Gen3 x16 Interface

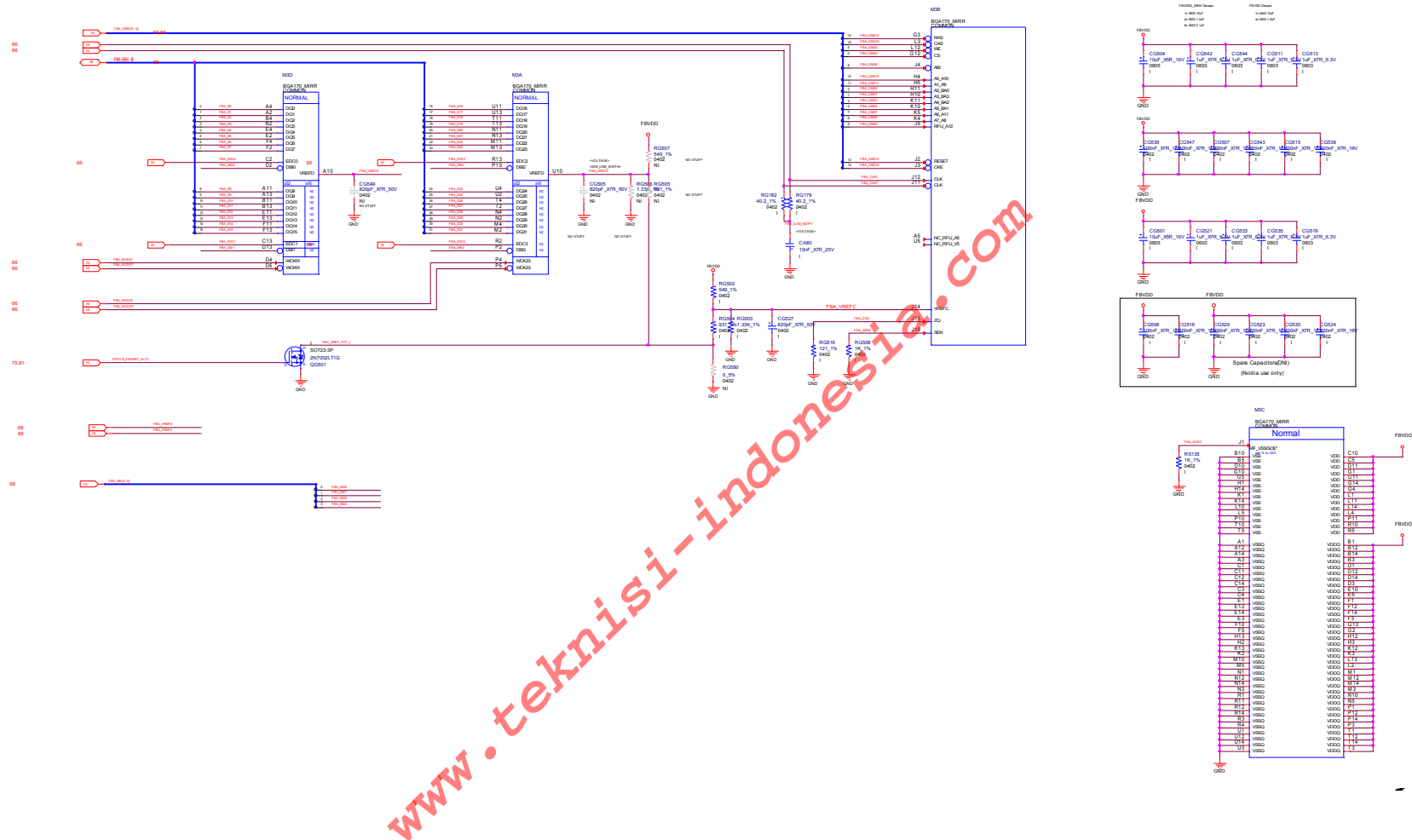


4. Frame Buffer Partition A

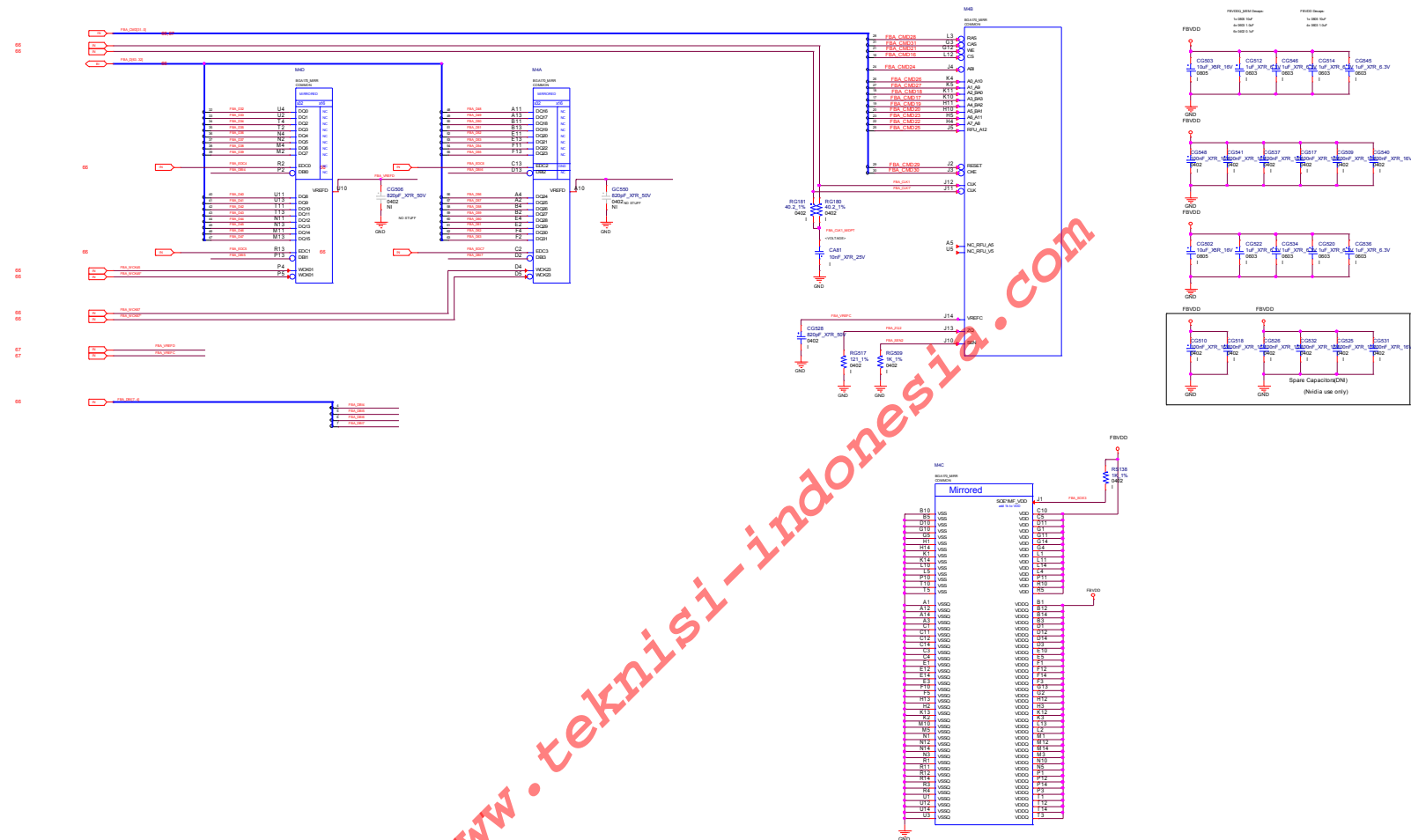
GOODS CMD Mapping Tab

<0.3s	<0.5s	MEMORY
12	28	RAS*
15	31	CAS*
5	21	WE*
0	16	CS*
8	24	AB*
10	26	A0_A10
11	27	A1_A9
2	18	A2_SA0
1	17	A3_SA3
3	19	A4_SA2
4	20	A5_SA1
7	23	A6_A11
6	22	A7_A8
9	25	A12_RFU
14	30	CWE*

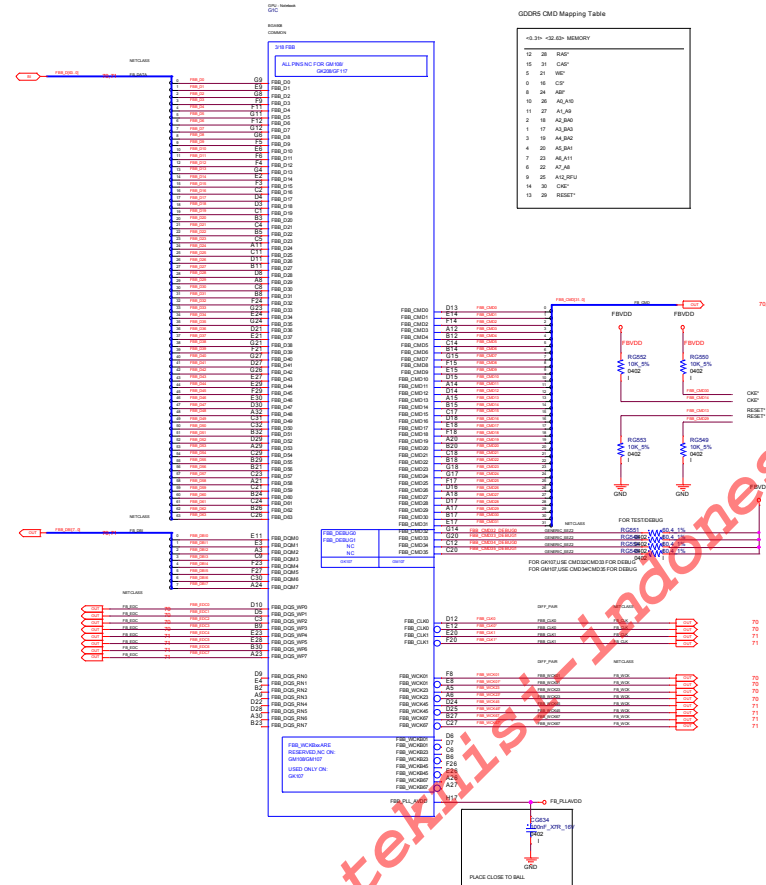
5. Frame Buffer Partition A - Lower Half

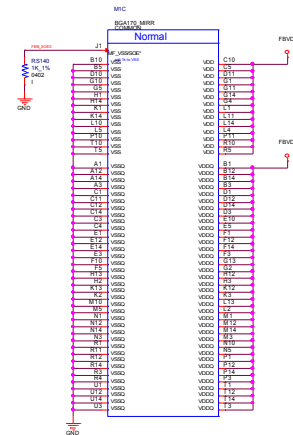
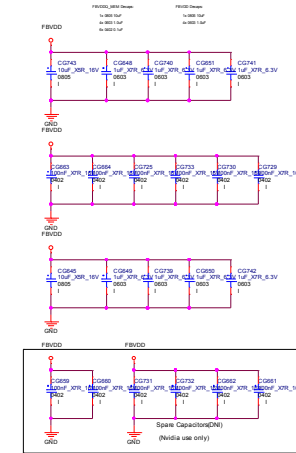


6. Frame Buffer Partition A - Upper Half

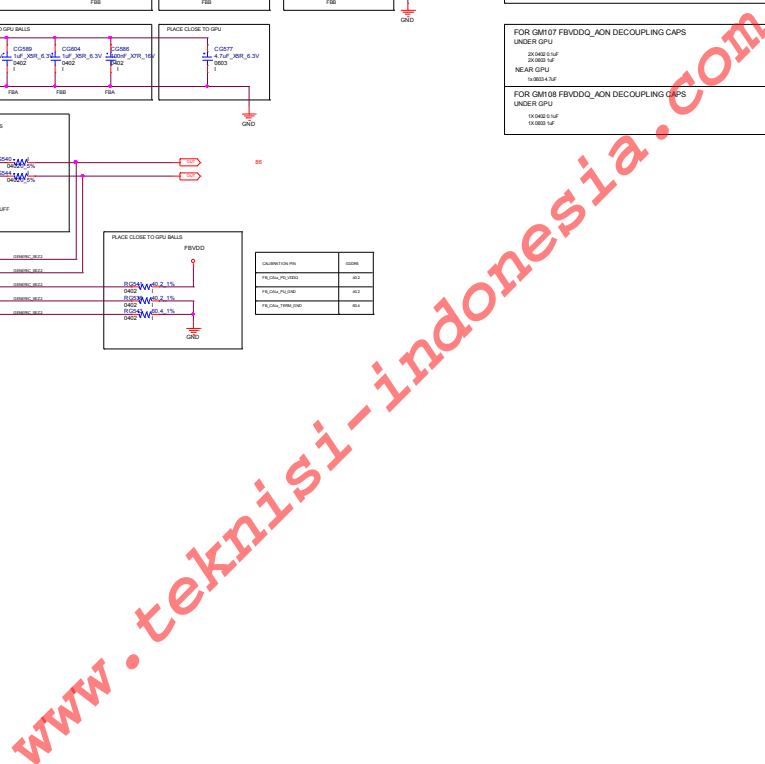


7. Frame Buffer Partition B



[illegible]

10. FBVDDQ Decoupling Caps



<p>FOR GM107 FIVDDQ_GPU DECOUPLING CAPS UNDER GPU</p> <p>1x 10K02 1.5F 2x 10K02 1.5F</p> <p>NEAR GPU</p> <p>1x 10K02 1.5F 1x 10K02 2.2uF</p>
<p>FOR GM108 FIVDDQ_GPU DECOUPLING CAPS UNDER GPU</p> <p>1x 10K02 1.5F 1x 10K02 1.5F</p> <p>NEAR GPU</p> <p>2x 10K02 1.5F 1x 10K02 1.5F 1x 10K02 2.2uF</p>
<p>FOR GM107 FIVDDQ_AON DECOUPLING CAPS UNDER GPU</p> <p>1x 10K02 1.5F 2x 10K02 1.5F</p> <p>NEAR GPU</p> <p>1x 10K02 1.5F</p>
<p>FOR GM108 FIVDDQ_AON DECOUPLING CAPS UNDER GPU</p> <p>1x 10K02 1.5F 1x 10K02 1.5F</p>

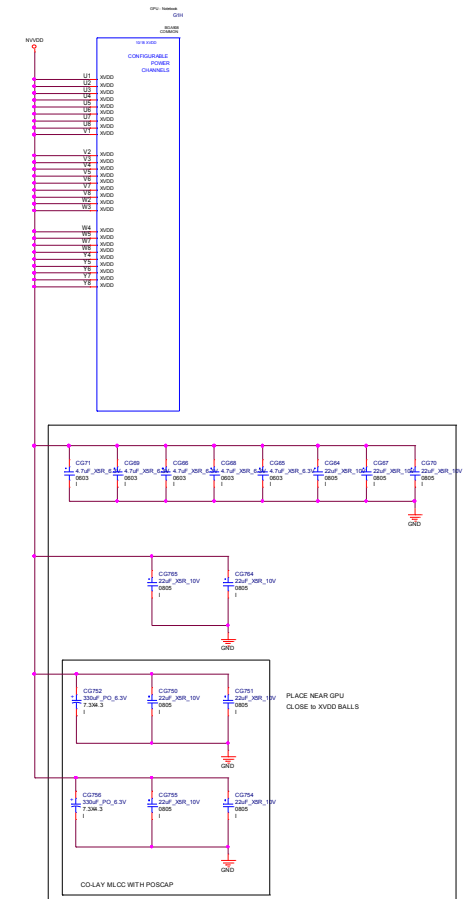
CALIBRATION PIN	DCOPR
FB_Cal ₁ _PD_VDDQ	43.2
FB_Cal ₁ _PU_SND	43.2
FB_Cal ₁ _TERM_SND	43.4

FOR GM108 DECOUPLING CAPS
UNDER GPU

4X 0402 1uF
10X 0603 4.7uF

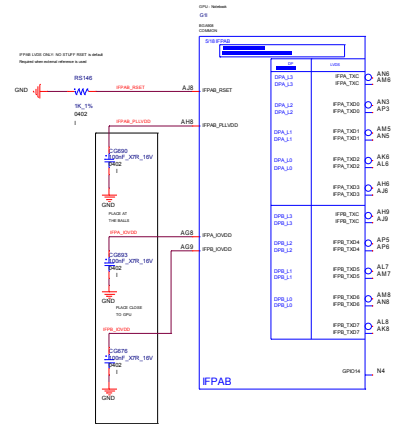
NEAR GPU

1x 0805 22uF
1x 0805 47uF
5x 0805 4.7uF
1x 7274 330uF



GM108 doesn't have display IO

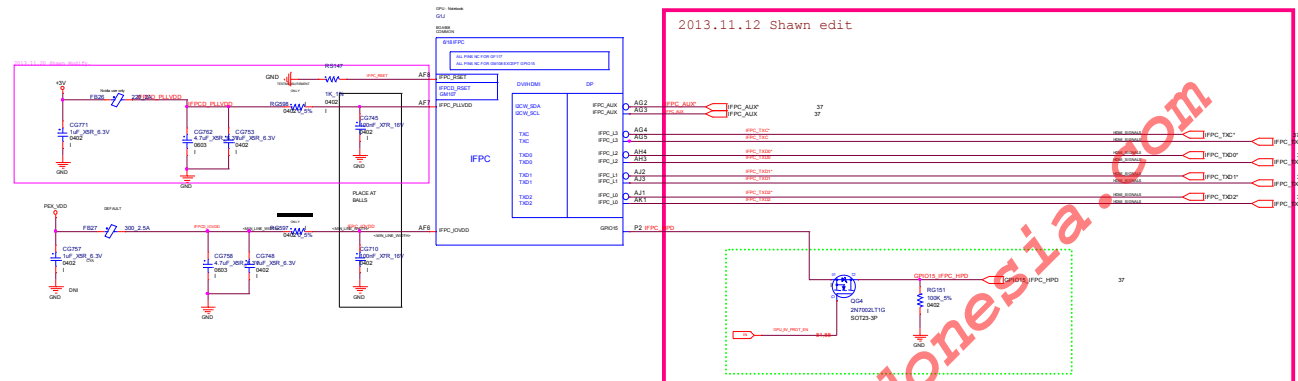
All IO section components will be No-o stuff



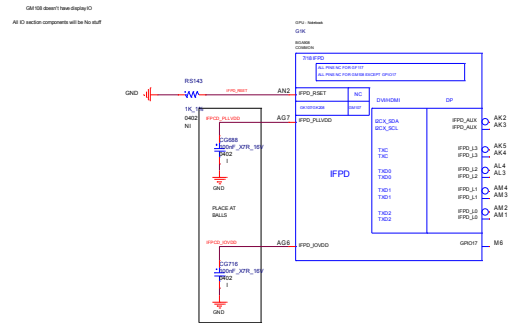
File		
IFPA_B 2xOPM		
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13. IFPC DPIIM

2013.11.12 Shawn edit: IFPC->IFPG

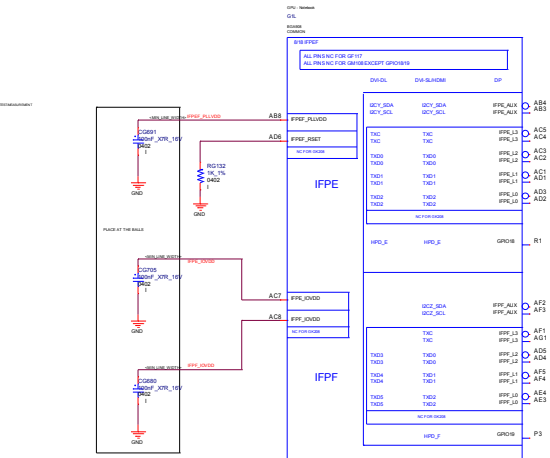


14. IFPD DPIIM



15. IFPEF DL-DVI

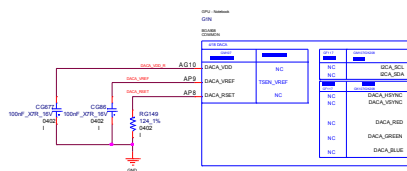
024108 Board/Frame Display 13
All IC section components will be 100 uAUF



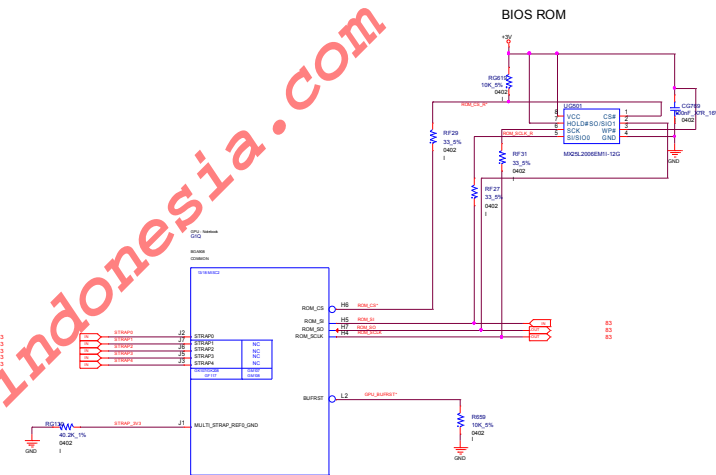
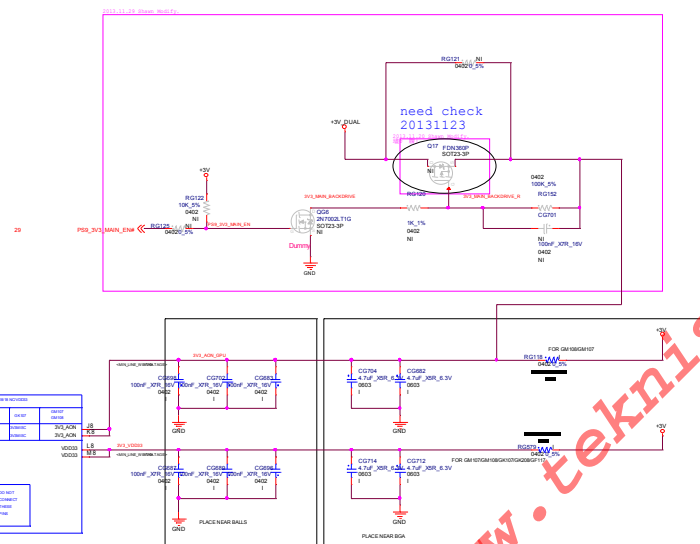
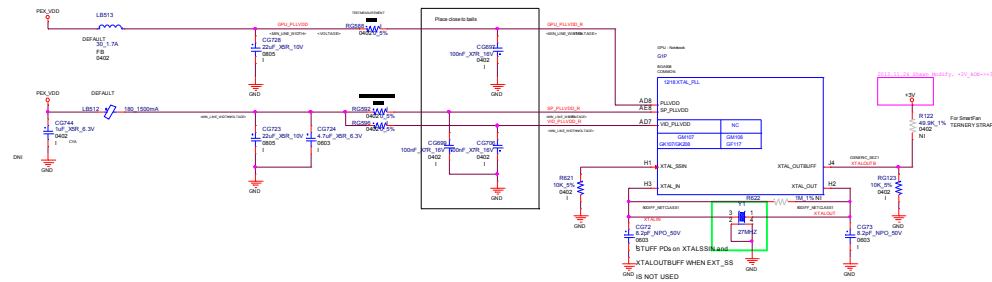
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[illegible]

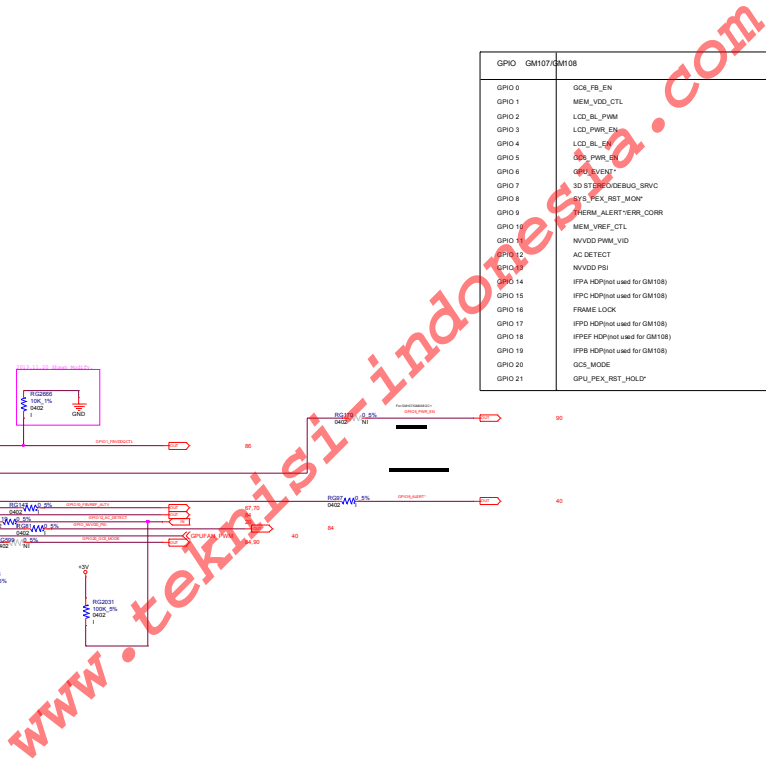
17. DACA



18. VBIOS ROM, XTAL, External SS and 3V3_AON/VDD33



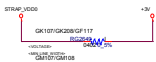
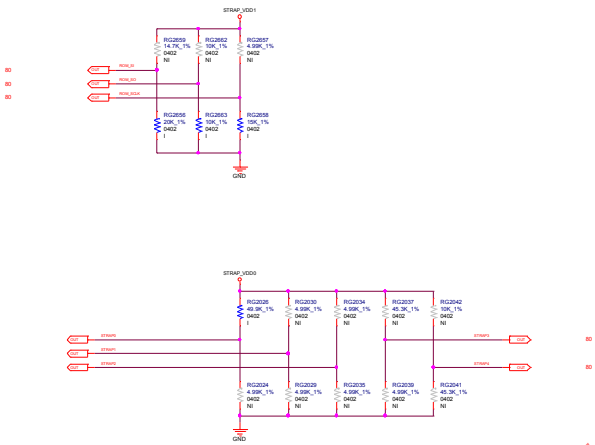
GM10X/GK10X STRAPPING MODE TABLE			
PIN NAME	MULTILEVEL	BINARY PRODUCTION	BINARY BRINGUP
MULTI_STRAP_REF_GND	49.2K TO GND	NOT SUPPORTED	NO STUFF



GPI0	GM107/GM108	GK20B/GK107
GPI0 0	GCS_FB_EN	FB_CLAMP_MON
GPI0 1	MEM_VDD_CTL	MEM_VDD_CTL
GPI0 2	LCD_BL_PWM	LCD_BL_PWM
GPI0 3	LCD_PWEN_EN	LCD_PWEN_EN
GPI0 4	LCD_BL_EN	LCD_BL_EN
GPI0 5	GCS_PWEN_EN	DEBUG_SRVC
GPI0 6	GCS_EVENT	FBCLAMP_TGL_REG
GPI0 7	IO STEREO/DEBUG_SRVC	3D STEREO
GPI0 8	GCS_FEX_RST_HOLD	OVER
GPI0 9	HERM_ALERT-ERR_CORR	THERM_ALERT-ERR_CORR
GPI0 10	MEM_VREF_CTL	MEM_VREF_CTL
GPI0 11	NVDD PWM_VDD	NVDD PWM_VDD
GPI0 12	AC DETECT	AC DETECT
GPI0 13	NVDD PS	NVDD PS
GPI0 14	IFPA HOPNot used for GM108)	IFPA+HOPFBCLAMP_TGL_REG
GPI0 15	IFPC HOPNot used for GM108)	IFPC HOP
GPI0 16	FRAME LOCK	FRAME LOCK
GPI0 17	IFPD HOPNot used for GM108)	IFPD HOP
GPI0 18	IFPF HOPNot used for GM108)	IFPF HOPNot used for GK20B)
GPI0 19	IFPS HOPNot used for GM108)	IFPS HOP
GPI0 20	GCS_MODE	NA
GPI0 21	GPU_FEX_RST_HOLD	NA

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PCI_DEVID5, PCI_DEVID4, & SUBVENDOR Strap Selectable

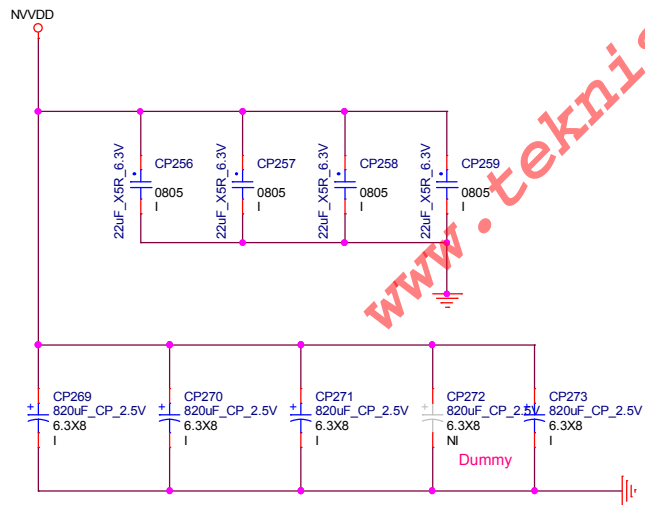
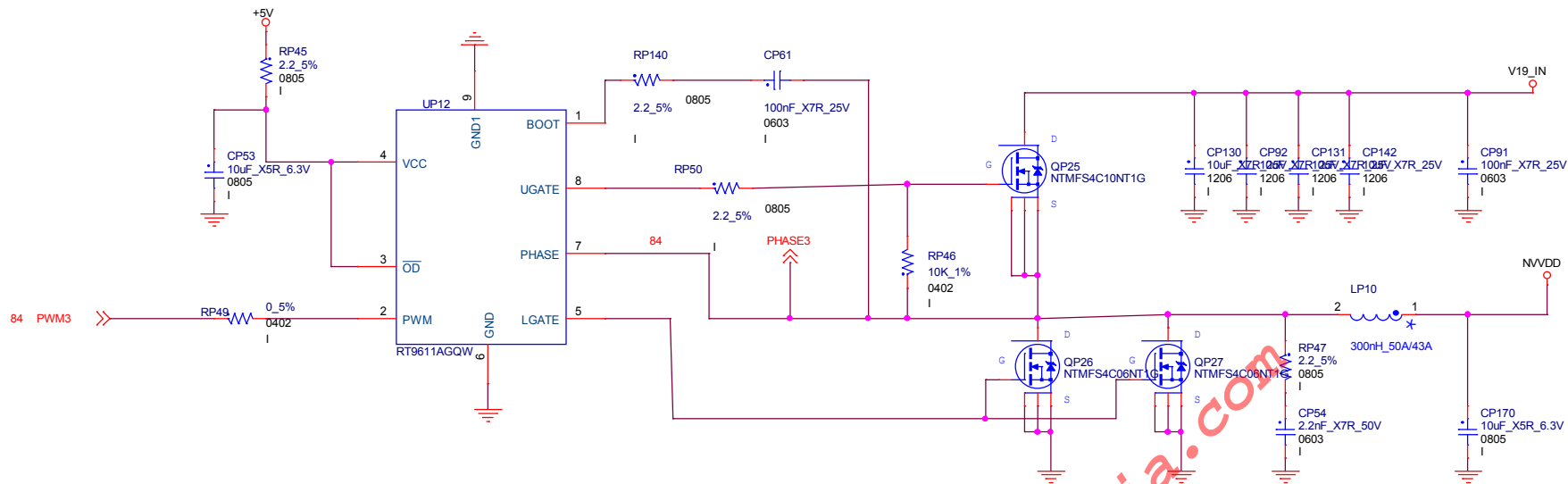


GK10X/208 STRAP PIN MODE TABLE	
PIN NAME	MULTI-LEVEL M [3-0]
STRAP0	USER[3:0]
STRAP1	3GIO_PADCFLG_AD[3:0]
STRAP2	PCI_DEVID[3:0]
STRAP3	SCM[3:0]_EXPOSED
STRAP4	PMIO_PIO_SPEED_CHANGE_DENI PCI_MAX_SPEED_DP_PULL_VDD33V
RCM_SCLK	PCI_DEVID[4:0] SUB_VENDID PCI_DEVID[0:3] PULL_PU_TERMIN0
RCM_S	RAMCFQ[3:0]
RCM_SD	FB[0] FB[0] SUB_ALT_ADDR VGA_DEVICE

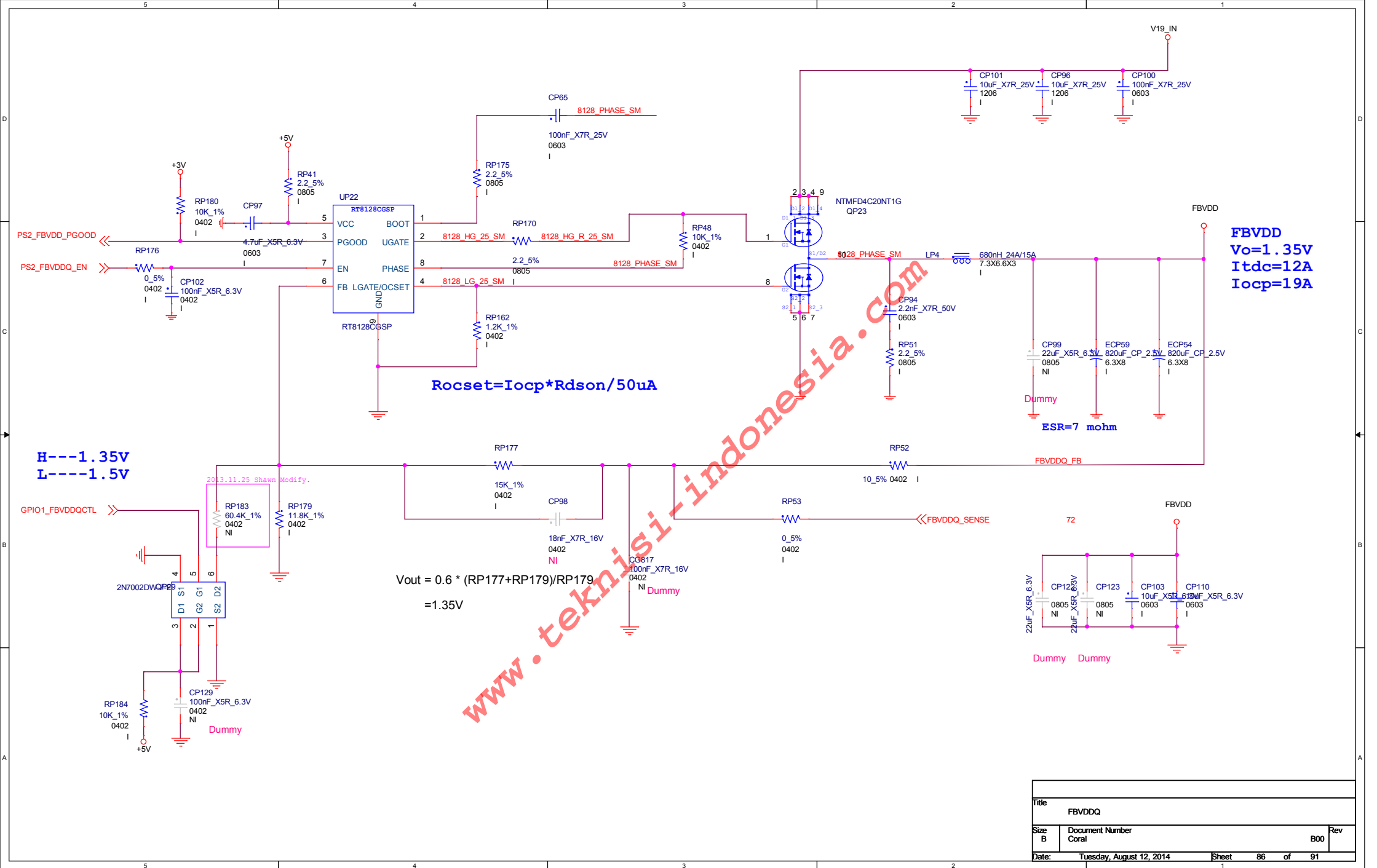
TERMINATION RESISTANCE	TERMINATION VOLTAGE	
	3V3 [3-0]	GND [3-0]
5K	1000 B	0000 B
10K	1001 B	0001 B
15K	1010 A	0010 B
20K	1011 B	0011 B
25K	1100 C	0100 B
30K	1101 D	0101 B
35K	1110 E	0110 B
40K	1111 F	0111 B

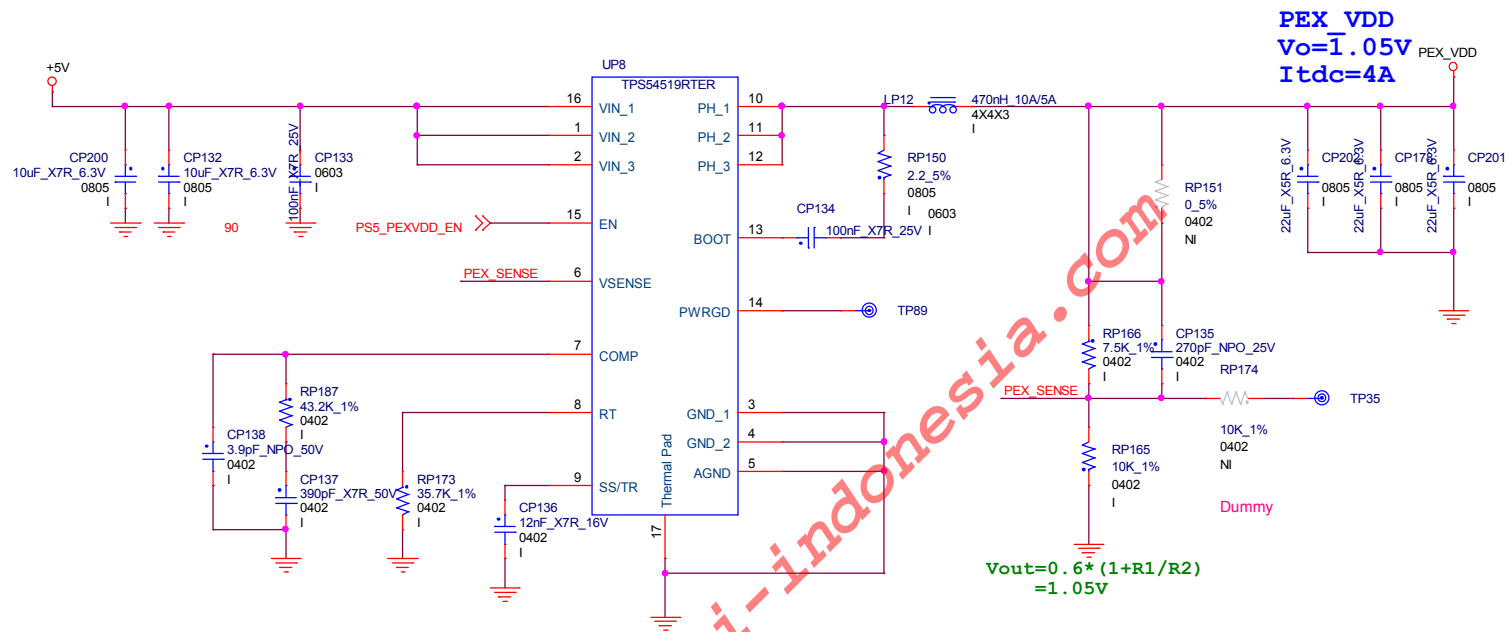
Configuration	Module	Strap	Strap	Manufacturer Part Number	Rev	Rev	Status
21041111 00000	00000	000	1-000	21041111-00000	000	0/0	00000
00000	000	000	1-000	00000000-000	000	0/0	00000

GM107/108 STRAP PIN MODE TABLE	
PIN NAME	MULTI-LEVEL M [3-0]
RCM_SCLK	SCM[3:0]_EXPOSED
RCM_S	RAMCFQ[3:0]
RCM_SD	DEVID_REL_PCIE_CFG_SMB_ALT_ADDR VGA_DEVICE
TERMINARY STRAP	
STRAP5	GDS Device[3:0] (Fm Delag[1:0] GDS Device[0:0])
XTAL_OUTLUFF	Smart Fan 33% PWM[3:0] Smart Fan 66% PWM[1:0] Smart Fan 99% PWM[0:0]



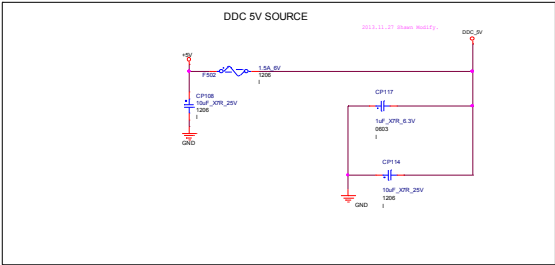
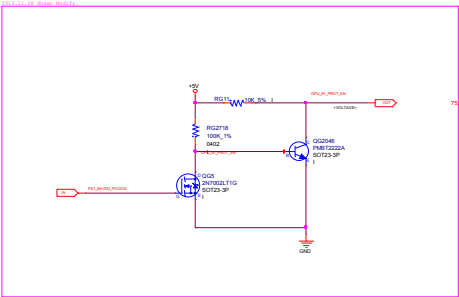
Title		
NVVDD driver		
Size	Document Number	Rev
B	Coral	B00
Date:	Tuesday, August 12, 2014	Sheet 85 of 91





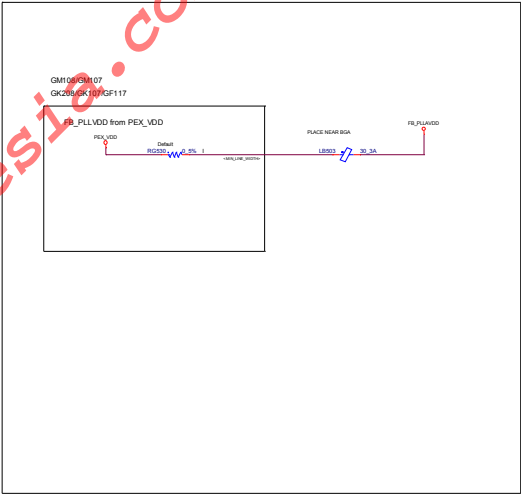
Title		
PEX_VDD1.05V		
Size	Document Number	Rev
B	Coral	B00
Date:	Tuesday, August 12, 2014	Sheet 87 of 91

27. Miscellaneous Voltage Rails

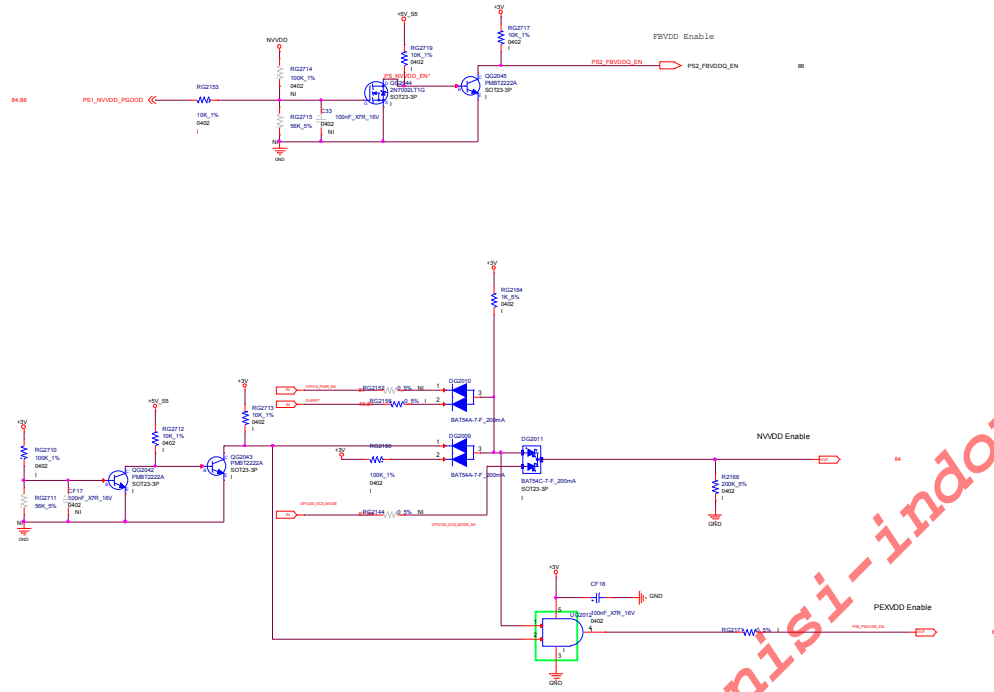


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28. PEX_VDD Switcher



30. Power Enables-1



2013-11-22 Changelist:
1140:
update J103, UV1, UV2, UV3, UV4, UV5, UV6, UU14, UU15,
PWR_STICH1, F_USB2_2, U502, U4, USB3.0_REAR3, NIC, M1, footprint

1730:
update DC power part.
modify J103\NIC\U4 symbol

1910:
update DC power part.
modify J103\NIC\U4 symbol

update MI footprint to BGA_0170_P080_140X120. need modify M1 symbol.
update P.12, P.22, P.26
update P.12 again.

2000 changelist:
Coral USB分段超长Issue:
update page48 delete UU12, add D1\D2\D3\D4.
update page39 delete UU9, add D5\D6\D7\D8.

update P.32 NIC symbol
update P.38 U4 symbol

1123-0900:
update P70 FBB EDC3/2 FBB DBI3/2
update P39 UU14/UU15 symbol
update P36 UV1/UV2/UV3/UV4/UV5/UV6 symbol
update P80 Q17 symbol
update P80 change UG501 from WINBOND to SST.

1123-1400:
update MI footprint to BGA_0170_P080_140X120. need modify M1 symbol.

1123-1500:
UPDATE P.59 CPU PROCHOT# change to H_PROCHOT#
update P.70 VDDQ(Pin B1) named:FBVDD
delete P.34 CHASSIS SPEAKER. INT_SPKR1 etc.

2013-11-25
1125-0900:
update P.12

Coral B00 => X00 Schematic and Layout Change log									
Instructions (click "*" to left if instructions are not shown.)									
#	Date	Page	Coral	Coral	Coral	Originator	Class	Description	Reason
20	1	19-Nov	29			Shawn Chang		Add Q_V5_ALW_MON Pull-high	
21	2		35			Shawn Chang		Close GND18 to PCE_MMIO_CPE_DETECT#	
22	3		23			Shawn Chang		Add VGA	
23	4		40			Shawn Chang		Modify EC01.EC02--10uF	
24									
25	5	20-Nov	81			Shawn Chang		Add +5v close to +3v	
26	6		31			Shawn Chang		Close VDD033 to Pin 11 and 32	Robin feedback.
27	7		33			Shawn Chang		link SPOFOUT and Pin1	Robin feedback.
28	8		33			Shawn Chang		Add DO2	Robin feedback.
29	9		34			Shawn Chang		Add R210-R213	Robin feedback.
30	10	21-Nov	32			Shawn Chang		Add RL35 0 Ohm	Kevin modify.
31	11		39			Shawn Chang		Add RU32 0 Ohm	Kevin modify.
32	12		39			Shawn Chang		ECU 470uF replaced by 220uF CU12,CU13.	Kevin modify.
33	13		48			Shawn Chang		Add RU67 0 Ohm	Kevin modify.
34	14		32			Shawn Chang		Add FB20	EMC needs.
35	15	25-Nov	66-71			Shawn Chang		Modify FBVDDQ_MEM to FBVDD	Kimball feedback.
36	16		31			Shawn Chang		Add a 10Kohm to 3.3V standby.	Robin feedback.
37	14		32			Shawn Chang		+3V_SS--+3.3V standby	Robin feedback.
38	18		32			Shawn Chang		C2,C3,C30 Y5V--X5R	Robin feedback.
39	19		12			Shawn Chang		Mem_PWRGOOD "and" H_DRAM_PWRGD	For system memory GOOD indicate
40	20		29			Shawn Chang		Add B_47K_PVRGD close to PVRGD_3V	Robin feedback.
41	21		32			Shawn Chang		Add C4,C20,C38,c39	Robin feedback.
42	22		32			Shawn Chang		Redraw REGOUT figure	Robin feedback.

Coral B00 => X00 Schematic and Layout Change log									
Instructions (click "*" to left if instructions are not shown.)									
#	Date	Page	Coral	Coral	Coral	Originator	Class	Description	Reason
20									
21	1	19-Nov	29			Shawn Chang		Add Q_V5_ALW_MON Pull-high	
22	2		35			Shawn Chang		Close GND18 to PCE_MMIO_CPE_DETECT#	
23	3		23			Shawn Chang		Add VGA	
24	4		40			Shawn Chang		Modify EC01.EC02--10uF	
25	5	20-Nov	81			Shawn Chang		Add +5v close to +3v	
26	6		31			Shawn Chang		Close VDD033 to Pin 11 and 32	Robin feedback.
27	7		33			Shawn Chang		link SPOFOUT and Pin1	Robin feedback.
28	8		33			Shawn Chang		Add DO2	Robin feedback.
29	9		34			Shawn Chang		Add R210-R213	Robin feedback.
30	10	21-Nov	32			Shawn Chang		Add RL35 0 Ohm	Kevin modify.
31	11		39			Shawn Chang		Add RU32 0 Ohm	Kevin modify.
32	12		39			Shawn Chang		ECU 470uF replaced by 220uF CU12,CU13.	Kevin modify.
33	13		48			Shawn Chang		Add RU67 0 Ohm	Kevin modify.
34	14		32			Shawn Chang		Add FB20	EMC needs.
35	15	25-Nov	66-71			Shawn Chang		Modify FBVDDQ_MEM to FBVDD	Kimball feedback.
36	16		31			Shawn Chang		Add a 10Kohm to 3.3V standby.	Robin feedback.
37	14		32			Shawn Chang		+3V_SS--+3.3V standby	Robin feedback.
38	18		32			Shawn Chang		C2,C3,C30 Y5V--X5R	Robin feedback.
39	19		12			Shawn Chang		Mem_PWRGOOD "and" H_DRAM_PWRGD	For system memory GOOD indicate
40	20		29			Shawn Chang		Add B_47K_PVRGD close to PVRGD_3V	Robin feedback.
41	21		32			Shawn Chang		Add C4,C20,C38,c39	Robin feedback.
42	22		32			Shawn Chang		Redraw REGOUT figure	Robin feedback.
43	23		34			Shawn Chang		PS1_NVDDQ_PG000 pull-high	Kimball feedback.
44	24		90			Shawn Chang		Change R02153 to 10K_1%,dummy R02714,R02715	Kimball feedback.
45	22-Nov	53				Kevin Peng		Update 1103 footprint	
46			36			Kevin Peng		Update UV1-6 footprint	
47	27		39			Kevin Peng		Update UU14,UU15 footprint	
48	28		48			Kevin Peng		delete UU12, add D1020D04	
49	29		70			Kevin Peng		delete UU9, add D506D708.	
50	28	23-Nov	70			Kevin Peng		FB20_EDC30 FBB_DB02	
51	31		39			Kevin Peng		UU14UU15 symbol	
52	32		36			Kevin Peng		UV10V20V30V40V50V6 symbol	
53	33		80			Kevin Peng		Q17 symbol	
54	34		80			Kevin Peng		change UG501 from WINBOND to SST	
55	35		49			Kevin Peng		CPU_PROCHOT# change to H_PROCHOT#	
56	38		70			Kevin Peng		VDDQ(Pin B1) named:FBVDD	
57	37		34			Kevin Peng		delete CHASSIS SPEAKER. INT_SPKR1 etc.	

1125-1540:
add P.91 changelist picture2.

1125-1840:
update SATA connector Footprint.

1126-0940:
change LP11.
P59: CP80 change to MURATA GRM155R60J105K CAP, 1uF, +/-10%,X5R, 6.3V, SMD0402, ROHS, HF
P53: RO91 part reference change to RP91
P59: RO96 part reference change to RP96

1126-1200:
TaiBei update
update P.24 Battery1 ;
update P.37 U10 Mfg PN:TS3DV642A0RUAR
delete P.65 RG557 and 3V3_MAIN.
update P.39 UU14 / UU15 (new symbol apply OK.)
update P.36 UV1/UV2/UV3/UV4/UV5/UV6 (new symbol apply OK.)
update P.39 USB3.0_REAR2/USB3.0_REAR3 (new symbol apply OK.)
update P.32 change LP11 size small.

1126-1400:
update P.83 table
update P.49 AlienHead footprint.
update P.49 LOGO header footprint.

1126-1900:
update P.32 replace LP11 to FB29
update P.42 BT link to P20 PCH GRI052.
update ALIEN HEAD footprint.
update P.88 Replace F502

1126-2130:
update UM6 footprint.

1127-0900:
update P.36 net DDC_5V

1127-1310:
update P.23 J104 for debug;
update RM15 and RM14 net name.

1127-1450:
update CG72 and CG73 from 20pF to 15pF.

1127-1850:
P.39 update! CU12,CU13 replaced by ECU6!
update P.87 EMC check result.

1127-1990:
update P.37 modify DDC_5V to DDC_5V_HDMI.

1127-2030:
update UV4 Pin7 net name;
change Pin L1/L2 to Pin M2/M3;
update UM6 symbol Pin number.

1128-1000:
update LP12
update MIN_LINE_WIDTH and VOLTAGE

1128-1730:
update RP57
p84 add CPP11
update LP12
P36 add 0.1uF for HDMI (EMC)
update Battery and Battery Connector

0425-2014:
Change RS225 from 1K to 10K, RO82 from 20K to 59K , RO78 from 1K TO 3K;